An integral path self-calibration scheme for a 20.1-26.7GHz dual-loop PLL in 32nm SOI CMOS

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Abstract

A bandwidth self-calibration scheme is introduced as part of a 20.1GHz to 26.7GHz, low noise PLL in 32nm CMOS SOI. A dual-loop architecture in combination with an integral path measurement and correction scheme desensitizes the loop transfer function to the VCO's small signal gain variations. The spread of gain peaking is reduced by self-calibration from 2.4dB to 1dB, when measured at 70 sites on a 300mm wafer. The PLL has a measured phase noise @10MHz offset of -126.5dBc/Hz at 20.1GHz.

Introduction

The phase noise and jitter transfer characteristics of high frequency (>20GHz) PLLs are critical to generating the required clocks in next generation wireline and millimeter wave applications [1]. This work presents novel techniques which are demonstrated to stabilize a PLL's loop transfer function in the presence of manufacturing variation. In a conventional analog PLL, in which the VCO's analog varactor is a small fraction of the VCO's total capacitance, manufacturing variations in the fixed (or digitally switched) capacitors must be compensated with large relative changes in the analog varactor voltage in order to achieve lock. This uncertainty affects the PLL's low frequency phase noise and jitter transfer function, because it is unknown a priori where on the non-linear VCO tuning curve the PLL will acquire lock. Consequently the VCO's small signal gain will be susceptible to process and temperature variations. In contrast, in a dual-path PLL (i.e. a PLL with separate integral and proportional control paths), this gain variation only affects the integral path. Once the PLL is in lock, the proportional control voltage remains close to the center of its range on the same part of the VCO tuning curve, irrespective of the output frequency. However, the integral path gain still varies due to the VCO varactor's non-linearity, which leads to uncertainty in the position of the first zero in the PLL's open loop response. The position of this zero plays a crucial role in suppressing close-to-carrier VCO noise (typically up-converted flicker nose). We present a technique in which the gain of integral path is calibrated allowing for the transfer function of the PLL to be more tightly controlled.

In [2] a technique for calibrating PLL dynamics is demonstrated, based, in part, on measuring the time in reference cycles for the PLL's phase error to cross zero in response to an injected phase step. However, in order to use this scheme to calibrate a PLL's small signal parameters the added phase step must be sufficiently small so that the perturbation to the loop is small-signal, and sufficiently large that the results are not corrupted by PLL phase offsets. These limitations make the scheme impractical for use in many PLLs including the dual-path design reported here.

In a PLL optimized for low noise, the VCO's analog tuning range per band is minimized in order to reduce the use of low Q varactors. Furthermore, in this dual-path PLL the proportional path varactor, which does not need to support a wide tuning range, is reduced to a fraction of the size of the integral path varactor (the proportional path resistor is increased to maintain the same loop gain). As a consequence, injecting phase steps into the loop can easily move the proportional control voltage sufficiently far from its steady-state position that the resulting response is not indicative of the small signal gain of the proportional path. Consequently, it is crucial to keep the injected phase step as small as possible. In addition, an analog PLL will have an input phase offset (due to charge pump current mismatch, loop capacitor leakage, etc.). Therefore, the time at which a PLL's reference and feedback clocks cross each other (measured with a bang-bang PFD) after a phase step has been injected, corresponds to the time taken to reach the PLL's offset, not the time when the PLL's phase crosses zero. Broadly, in a low noise dual-path PLL, large phase step-based measurements are corrupted by non-linearities, and small phase step-based measurements are corrupted by phase offsets.

To avoid these limitations, a novel integral path self-calibration algorithm is included in the PLL, as shown in block diagram form in Fig. 1. The key elements of the algorithm include temporarily disabling the proportional path from the time when a phase step is applied to the time crossover is detected and aggregating crossover information from phase steps of opposite signs to eliminate the offset error. A digital state machine performs the integral path self-calibration. This state machine monitors the lock and crossover detectors, and controls the feedback divide ratio and integral path gain. Self-calibration starts once the on-chip lock detector detects lock. Firstly, a phase step is added to the loop, by temporarily changing the count value in the feedback divider, while simultaneous disabling the proportional path (similar to [2]). The time (in clock cycles) until the output of the bang-bang phase detector switches polarity is measured, after which the proportional path is re-enabled and the PLL is allowed to re-lock. Next, the measurement is repeated with a phase step of opposite polarity. The average of these paired time-to-crossover measurements is independent of the PLL's offset (this independence does not generally hold for a PLL's response to opposite polarity phase steps, it only holds when the proportional path is disabled). The calibration state machine then moves the averaged time-to-crossover value to a target value, by incrementing or decrementing the integral path gain, and re-measuring until the target is reached. The integral-path gain is controlled via the charge pump current and capacitor value.

The dual-loop PLL includes separate fully differential proportional and integral control paths. Fig. 3 shows the details of the dual control paths. The charge pump currents and loop filter resistors and capacitors can be independently digitally programmed. The PLL consumes a total of 33mW (excluding input and output buffers. The PLL locked over a 20.1 – 26.7

GHz frequency range; Fig. 2 shows the PLL's locked phase noise performance.

Measurements

In order to demonstrate the effectiveness of the integral path self-calibration system, the PLL's in-band phase noise, shown at the top in Fig. 4, and loop transfer function, shown at the bottom, were measured at 9 different frequencies equispaced from fastest to slowest in a single coarse tuning band. On the left are the measurements without self-calibration, which show significant variation in both phase noise and transfer function, due primarily to varactor non-linearity. On the right are the phase noise and transfer functions measurements after self-calibration, which demonstrates a dramatic reduction in the variation of in-band measured phase noise and loop transfer function. In a second test of the integral path self-calibrating PLL, the 3dB bandwidth and jitter peaking were measured at a fixed output frequency (25GHz) across an entire wafer. The results of this test, plotted in Fig. 5, show that the spread of jitter peaking is reduced from 2.4dB to 1dB.

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References

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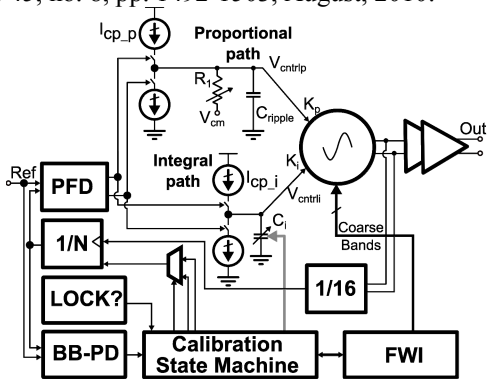

Figure 1: Simplified block diagram of the PLL.

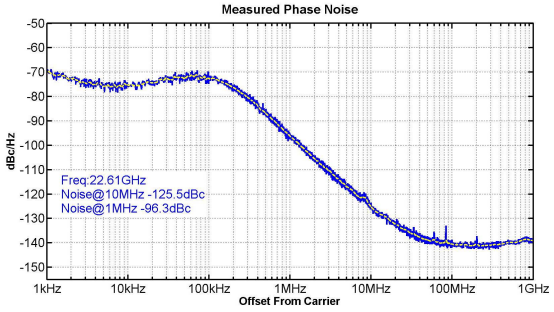

Figure 2: Measured phase of the PLL at 22.61GHz was -125.5 @10MHz offset

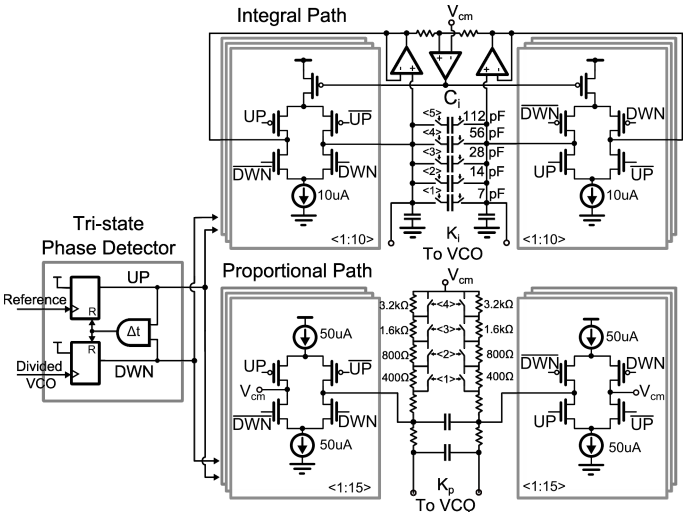

Figure 3: Details of the proportional and integral charge-pumps and filters.

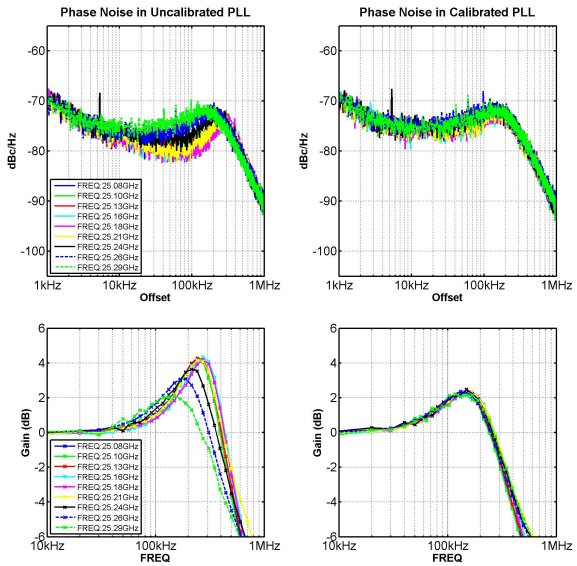

Figure 4 : Top: In-band phase noise before and after self calibration. Bottom: Measured PLL transfer function before and after calibration

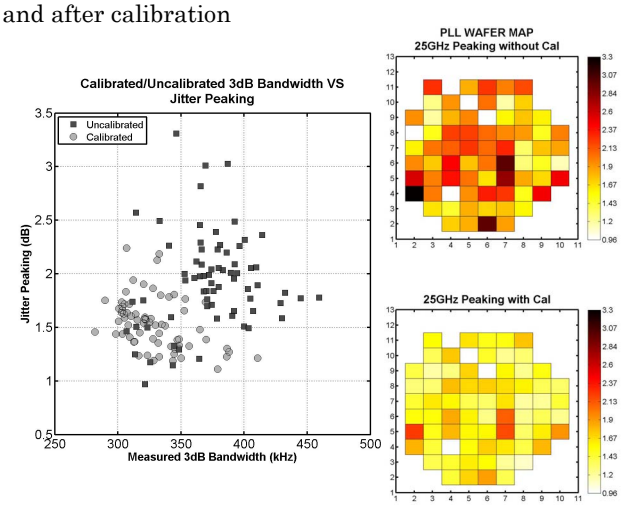

Figure 5: Measured 3dB bandwidth and jitter peaking before/after calibration. Measurements made on every functioning die on a 300mm wafer