Optical Waveguides and Photodiodes in 0.18µm CMOS SOI with No Post-processing

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Abstract: We demonstrate the first optical waveguide and fastest photodiode implemented in a commercial CMOS technology without performing any post-processing. The measured waveguide loss at 1.55µm is 37dB/cm and bandwidth of photodiode exceeds 9.2GHz at 850nm.
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1. Introduction

CMOS technology has revolutionized the electronic industry over the past few decades by the sheer force of transistor scaling, unmatched levels of integration, low cost, and high yield. Reliable fabrication processes, accurate modeling, and predictable behavior of CMOS integrated circuits have significantly reduced the cost of complex electronic systems. Inspired by the success of CMOS technology, the field of silicon photonics has attracted a lot of attention during the last several years. The main goal has been reducing the cost and improving the overall system performance by integrating electronic and photonic components on the same chip [1]. Recently, many leading groups in academic institutions and industry have fabricated and reported ″CMOS-compatible″ optical components but there are several major challenges that must be addressed. First, while many fabrication processes and optical devices are denoted as CMOS compatible, the true CMOS process technology offered by major foundries are highly optimized to enhance the electronic performance of transistors and designers do not have any control over the process steps. Second, fabrication and yield considerations restrict the width, thickness, and spacing of various layers such as silicon, oxide, and metal. Designers must obey these strict design rules and choose from a limited set of parameters, which is usually far from the optimal values for an optical device. In addition to the size limitation, other major challenges include mandatory metal filling and high-level of doping which significantly increase the propagation loss in integrated waveguides.

In this paper, we report optical waveguides and photo-detectors implemented in a conventional 0.18µm CMOS SOI process technology with no post-processing steps required. Recently several groups have reported optical waveguides in bulk CMOS [2,3] or thin buried oxide CMOS SOI process [4]. As these process technologies do not support a low-loss optical guiding mode, custom post-processing is required which increases the cost and reduces the yield of these chips. In this work, we have implemented optical waveguides and photodiodes in a conventional CMOS SOI process with buried oxide (BOX) thickness of 1µm. This thickness is large enough to suppress the leaky modes and allow a low-loss guiding mode without any need for post-processing. In addition to the waveguide, high-speed photodiodes are implemented. The 1µm BOX layer inherently blocks the slow diffusion current, boosting the speed of the photodiode tremendously. The waveguides and photodiodes are implemented in IBM's 0.18µm CMOS SOI process technology [5]. As design rules impose default metallization and doping steps, specific blocking layers are added above the optical components to minimize the waveguide loss. The strict design rules also enforce local and global minimum pattern densities and metal fills are routinely added during the fabrication process to satisfy these requirements. Since metal fills near or above the optical waveguides significantly increase the loss of these waveguides, dummy metal layers are carefully added to meet the density requirement without affecting the waveguide loss.

2. Optical waveguides

The core of the waveguide is implemented using the active and polycrystalline silicon layers as shown in Figure 1(a). The core region has a width of 400nm and height of approximately 300nm. Four waveguides with lengths of 0.5mm, 1mm, 1.5mm, and 2mm are implemented. All waveguides have an identical 90º bend section with radius of approximately 50µm. Grating couplers are integrated in the input and output of the waveguides. Since designers cannot control the height of the silicon layer, it is not possible to adjust the teeth depth of the grating coupler to any desired value. Based on the simulations results and to maximize the coupling efficiency, the grating coupler is implemented by fully-etched gaps filled with oxide, where in the gap no silicon is preserved.

Figure 1(b) shows the measured results of the normalized received power for a fixed transmitted power. The waveguide loss is evaluated to be 37dB/cm. In the previously published CMOS optical waveguides, authors reported loss numbers from approximately 55dB/cm to sub 10dB/cm after post-processing steps, and 500dB/cm or even higher without these steps [2-4]. To the best of our knowledge, the reported loss in this paper is the lowest among all published CMOS optical waveguides that did not utilize post-processing.

Two major factors that contribute to waveguide loss are identified. The first one is edge roughness of the silicon layer. According to [6] the waveguide loss scales quadratically with the edge roughness. In [7], edge roughness of 9nm resulted in more than 30dB/cm loss for similar waveguide sizes. As the edge roughness in 0.18μm CMOS technology node is estimated to be several nm [8], it is likely that edge roughness contributes a significant portion to the total loss. The second factor that contributes to loss is the use of polycrystalline silicon as part of the waveguide core. It is known that polycrystalline silicon introduces higher loss than single-crystalline silicon.

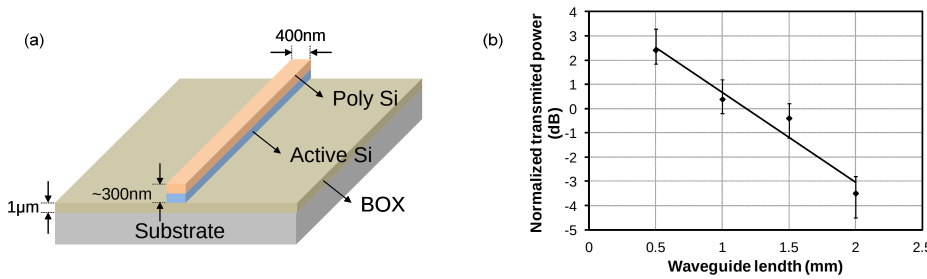

Figure 1: (a) Waveguide structure (Surrounding oxide is not shown here). Dimensions are not drawn to scale. (b) Waveguide transmitted power vs. waveguide length at 1.55μm.

3. Photodiodes

Integration of photodiodes in a conventional CMOS technology provides exciting opportunities for implementing optical receivers. Compared to photodiodes implemented in bulk CMOS processes where the bandwidth is severely limited by the diffusion current generated deep in the substrate, photodiodes implemented in this work have inherently larger bandwidth as the BOX layer blocks slow carriers generated in the substrate. In this work, we investigate important parameters of a photodiode including bandwidth and photoresponsivity. Various photodiode geometries are implemented and their performance is studied.

The photodiodes reported in this paper are lateral N-well/P+ diodes. In this work, a directly-modulated 850nm Vertical-Cavity Surface-Emitting Laser (VCSEL) is used as the source. The optical beam is collected using multimode fibers and then coupled to the photodiode vertically. The optical power is fixed at -13dBm. VCSEL and photodiodes are biased externally using high-frequency bias-tees. The RF ports of these bias-tees are used to modulate the VCSEL laser and collect high-frequency response of the photodiode. The frequency response of the photodiodes is measured using Agilent network analyzer N5230C.

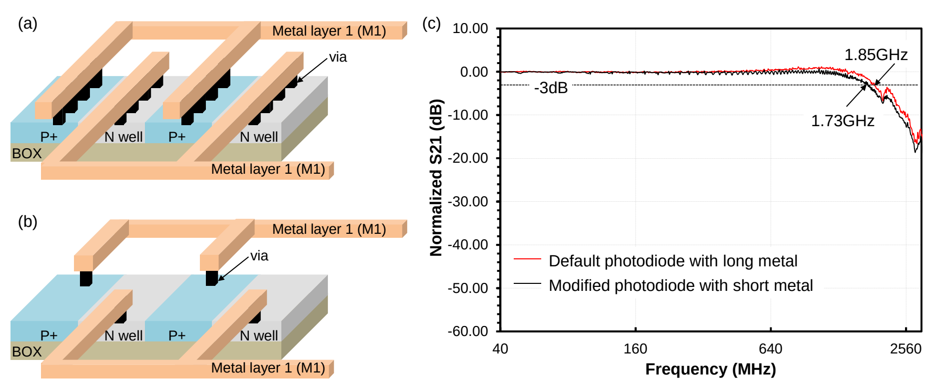

Figure 2: (a) and (b) are simplified layouts for photodiodes with long and short metal, respectively. Dimensions are not drawn to scale. (c) Effect of the metal layers on the bandwidth of photodiodes.

The effect of the M1 metal layer on the bandwidth of the photodiodes is studied. In all of the default diodes provided by the foundry, the M1 metal layer covers the whole N-well/ P+ region to minimize the ohmic loss of the metal contact, as shown in Figure 2(a). Multiple vias are placed between the metal and the N well/ P+ region to collect the current and further reduce the resistance of the contact. Although using more metal contacts improves the frequency response of the electronic diodes, it also degrades the photoresponsivity by blocking some of the incident photons. In order to increase the photoresponsivity, the layout of the default photodiodes is modified by removing a large portion of the M1 layer from the top of the photo-diode, as shown in Figure 2(b). Two versions of the photodiodes (default and modified) with size of 50µm by 50µm are implemented. It is observed that at reverse-bias of -3V, the photoresponsivity of the modified photodiode (removed M1) is about two times larger than that of the default one. The measured photoresponsivities of the default and modified photodiodes are 0.02A/W and 0.04A/W, and their bandwidths are 1.73GHz and 1.85GHz, respectively, as shown in Figure 2(c). This slight degradation in bandwidth is due to higher path resistivity, which causes a larger RC delay and a smaller electrical field in the depletion region. At reverse bias of -10V, the difference between two photodiodes is consistent with that at low voltage. The responsivity and bandwidth are 0.05A/W and 2.3GHz for the default photodiode, compared to 0.1A/W and 1.87GHz of the modified one.

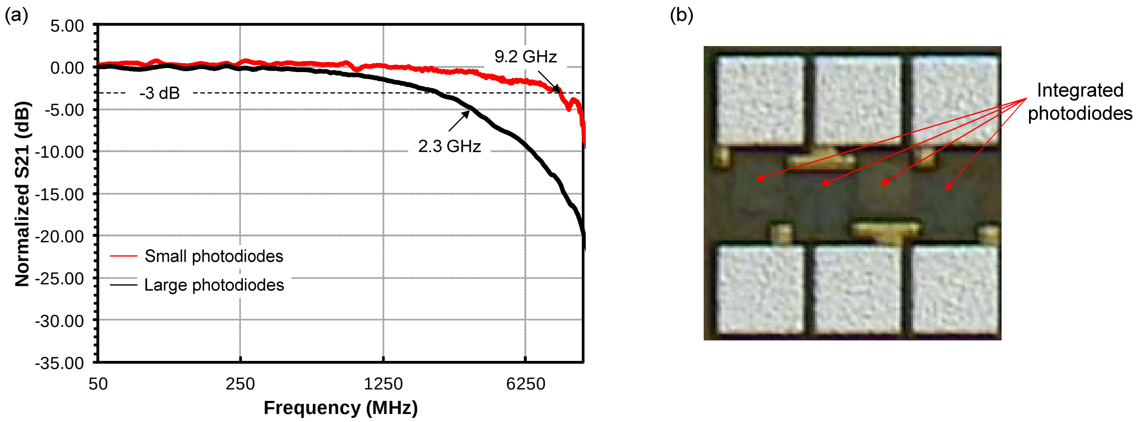

Figure 3: (a) Effect of the physical dimensions on the performances of photodiodes. (b) Micrograph for the photodiodes with bondpads.

We next report the effect of diode size in its photoresponsivity and frequency response. In Figure 3(a), the bandwidth of two photodiodes with dimensions of 50µm×50µm and 10µm×10µm are compared. Both photodiodes have long metals (default diodes). A reverse bias of -10V is used in this measurement to push the photoresponsivity. The measured photoresponsivity of the small and large photodiodes are 0.008A/W and 0.05A/W, respectively. The measured -3dB bandwidth of the small diodes is four times larger than that of the large diodes. A micrograph of the photodiodes is shown in Figure 3(b).

4. Conclusion

In this work we reported the performance of optical waveguides and photodiodes implemented in a conventional 0.18µm CMOS SOI process technology. The waveguide loss was 37dB/cm at 1.55µm, which is the lowest number among all reported CMOS optical waveguides that did not use any post-processing. The effects of the M1 metal layer and physical dimensions of the photodiode were also reported. At wavelength of 850nm, maximum photoresponsivity of 0.1A/W and -3dB bandwidth of 9.2GHz were achieved for -10V reverse bias.

5. References

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