Sub-picosecond Wireless Synchronization Based on a Millimeter-Wave Impulse Receiver with an On-chip Antenna in 0.13µm SiGe BiCMOS

Babak Jamali and Aydin Babakhani

Rice University, Houston, TX, United States

***Abstract* — This paper presents a wireless synchronization receiver using sub-8psec pulses. A novel self-mixing technique is introduced to detect low-power picosecond impulses and extract the repetition rate with a low timing jitter. The chip is fabricated in a 0.13µm SiGe BiCMOS process and achieves a time transfer accuracy of 376fsec. The receiver, which is integrated with a broadband on-chip antenna, successfully detects a picosecond pulse train with a 3.1GHz repetition rate and generates an output locked to this rate with a phase noise of -89 dBc/Hz at 100 Hz frequency offset. The chip consumes 146 mW from a 2.5V supply and occupies an area of 1.89mm^2.**

Index Terms — Impulse receiver, millimeter-wave, nonlinear circuits, timing jitter, wireless synchronization, SiGe, BiCMOS.

I. Introduction

Wireless synchronization of a distributed array with widely-spaced sparse elements is a key enabler in coherent combining of signals in space. The angular resolution of an imaging array can be enhanced by increasing the aperture size of the array, which demands a precision synchronization link with a small timing jitter among the array elements. A wireless method for synchronizing multiple chips will ease the scalability of the array. Millimeter-wave Continuous Wave (CW) sources have been used for this purpose [1] but, in CW methods, time-varying channels in a multi-path environment adds Non-Line-of-Sight (NLOS) reflections to the received signal, which results in high phase and amplitude jitters. However, due to the difference in the travel time, LOS and NLOS signals at the receiver can be separated by transmitting ultra-short pulses via multiple antennas and utilizing spatial modulation techniques.

The authors in [2] introduced an oscillator-less direct digital-to-impulse radiator with a repetition rate of several GHz. Ringing effects generated by the trigger signal in [2] and the reflections caused by nearby objects (such as antenna packaging and DC biasing wires) introduce undesired zero-crossings that pose a serious challenge in extracting the repetition rate in the receiver. In this work, we present a novel mixer-based receiver with an on-chip antenna to remove the undesired ringing, detect the desired high-frequency components, and generate a reference signal locked to the repetition rate of the incoming pulse train. The operating frequency range of this system can potentially be much larger than narrow-band injection-locked based CW oscillators. The presented chip can detect pulses with a repetition rate of 1 to 10 GHz.

II. Proposed Architecture

Ultrashort impulses, such as those reported in [2], have a broad Gaussian-like continuous spectrum covering mm-wave and THz frequencies. When these impulses are generated with a fixed repetition rate, their frequency spectrum becomes a Gaussian-modulated comb. If these frequency tones are passed through a nonlinear block, self-mixing occurs and the frequency of the mixer output becomes equal to the repetition rate of the impulse train (see Fig. 1). It is important to note that due to the high-frequency contents of the impulse train, a simple linear filtering cannot be used to extract the repetition rate.

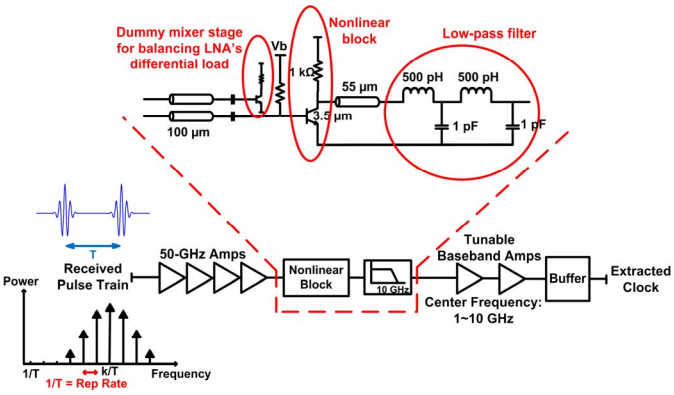

Fig. 1. Block diagram of the receiver, circuit schematic of the nonlinear block, and an example of a Gaussian pulse train in time and frequency domains.

The single-chip impulse receiver reported in this work consists of a broadband on-chip bow-tie antenna, a four-stage narrowband low-noise amplifier centered at 50GHz, a nonlinear block to perform self-mixing, a low-pass filter, and baseband amplifiers. Circuit schematics are illustrated in Fig. 1 and 2. The bow-tie antenna has a resonance frequency of 50 GHz (pulse center frequency). A silicon lens is used on the back of the chip to reduce the substrate modes caused by the substrate. The four-stage low-noise narrowband amplifier amplifies the received signal in the 40-60 GHz band and has a simulated peak gain of 28 dB. The amplified components are fed to an npn-based nonlinear block. The nonlinearity of this block can be controlled by varying the bias voltage (V_b) of the base. Because the goal is to perform mixing on multiple tones of a single signal and there is no high-power LO input

available, a conventional mixer, such as Gilbert cell, is not practical. In this design, the intermodulation products at the output of this mixer do not degrade the performance of the circuit because they have the desired repetition frequency or its harmonics. To reject the high-order harmonics, a 4th-order Chebyshev low-pass filter with a cutoff frequency of 10 GHz is used immediately after the mixer to attenuate the high-frequency components, as well as the direct coupling from the input.

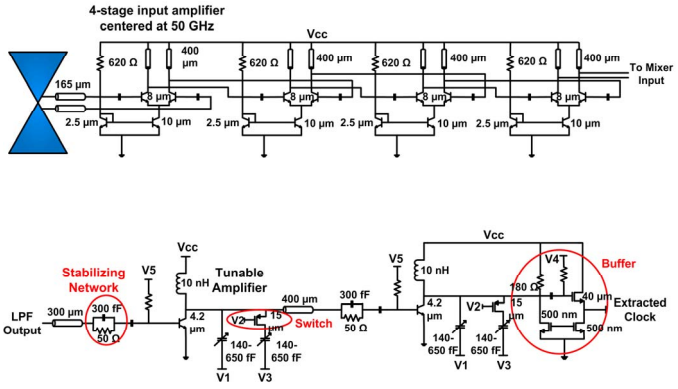

Fig. 2. Detailed circuit schematics of the input (top) and output (bottom) amplifier stages.

The receiver reported in this work has a tunable center frequency to extract a wide range of pulse repetition rates ranging from 1 to 10 GHz. This is achieved by using a two-stage tunable baseband amplifier to select the desired frequency component. Each stage uses an inductor in parallel with two branches of switched varactors to control the center frequency (see Fig. 2). The baseband amplifier has a simulated gain of 27.5 dB when tuned at 5 GHz. The output signal is then fed to a source follower buffer stage to drive a 50-Ω load.

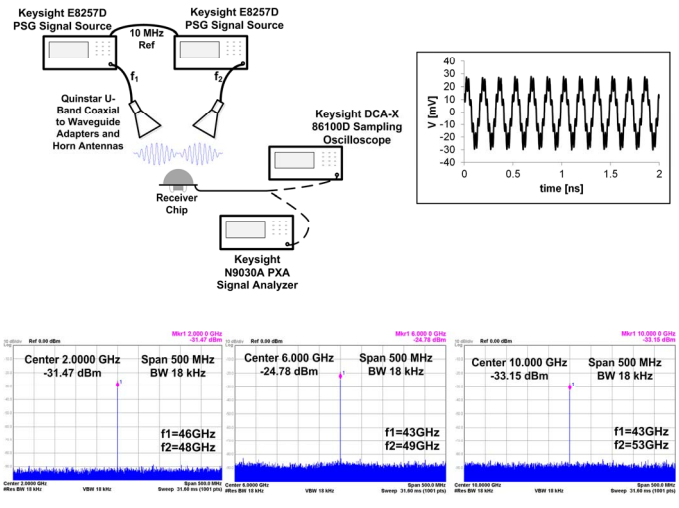

Fig. 3. Two-tone measurement setup (left), measured time-domain output waveform for 42 and 48GHz sources (right), measured output spectrum for three sets of frequencies (bottom).

III. Measurements

Two measurement setups have been used to characterize the performance of the chip. In the first setup (Fig. 3), two synchronized RF signal generators are used to produce two high-power frequency tones in the range of 40 to 50 GHz. These signals are then fed to horn antennas and combined in the air before arriving at the chip. The combined signal has a pulse-shaped waveform in the time-domain. Measurement results, including the output spectrum, phase noise and timing jitter, are shown in Figures 3 and 4. The output of the receiver chip indicates an rms timing jitter of 376fsec. This value is compared with the 360fsec timing jitter of the 48GHz source in the same figure. In this measurement, the power of the synchronized sources is set at 10 dBm. The receiver is placed at a distance of 10 cm from the antennas. Figure 5 reports the measured nonlinear behavior of the circuit, where the effect of the base voltage on the measured output power is described. In this measurement, the strongest second-order nonlinearity at an optimum base voltage of 0.87V is achieved. The right plot in Fig. 5 shows how the measured output power of the chip varies with the source power, demonstrating the linear behavior of the receiver.

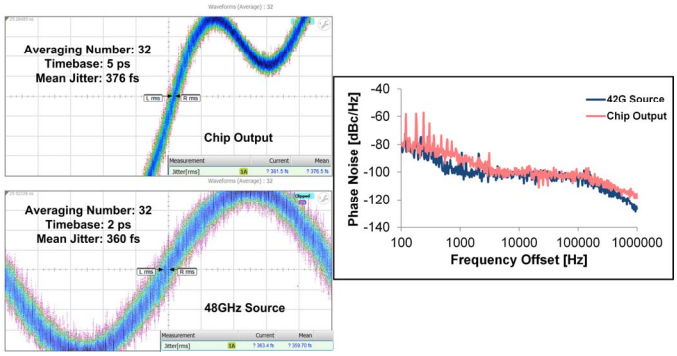

Fig. 4. Comparing the measured timing jitter of the output and the source (left), and a comparison between the measured phase noise of the 42G source and the 6GHz carrier at the output when f_1=42GHz, f_2=48GHz (right).

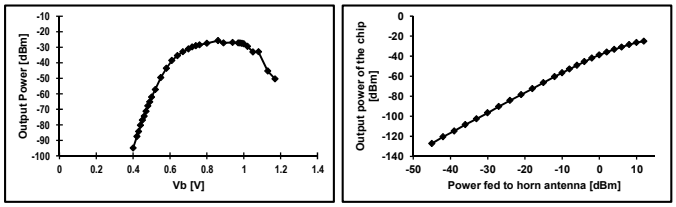

Fig. 5. Measured output power of the chip vs. the base voltage of the main bipolar transistor (left), and measured output power of the chip vs. the power fed to a 26dB horn antenna (located at a 10-cm distance) (right).

In the second measurement setup, shown in Fig. 6, an impulse-radiating chip is used to radiate a broadband ultra-short pulse train with a repetition rate of 3.1 GHz. The time-domain waveform of the radiated pulse train, measured by a

TABLE I

PERFORMANCE COMPARISON OF WIRELESS SYNCHRONIZATION CIRCUITS IN SILICON

	This Work	[1] CICC '15	[3] ISSCC '06	[4] JSSC '09	[5] IMS '14	[6] RWS '16
Time Transfer Method	**Picosecond Pulse**	Continuous wave	Continuous wave	UWB	Optical	Pulse
Technology	**0.13µm BiCMOS**	65nm CMOS	0.13µm CMOS	0.18µm CMOS	0.18µm CMOS	0.13µm BiCMOS
Phase Noise at 100Hz and/or RMS Jitter	**-89 dBc/Hz, 376 fs**	-70 dBc/Hz	5 ps (pk-pk jitter)	4.6 ps	-57 dBc/Hz, 1.6 ps	100 fs
Input Frequency	**30-100 GHz (8ps pulses)**	102.8-104.4 GHz	17-18.7 GHz	0.2-7 GHz (Pulse)	850 nm (Optical)	200ps pulses
Output Frequency Range	**1-10 GHz (widest range)**	51.4-52.2 GHz	2.135-2.337 GHz	3 GHz	1.295-1.381 GHz	<5 MHz
Measurement Distance	**10 cm**	5 cm	0.25 cm	0.05 cm	150 cm	5 cm
Die Area [mm^2]	**1.89 (with pads and antenna)**	6.46 (with PA and TX antenna)	1.14 (without pads)	2.34 (RX and antenna)	0.275	0.42 (with pads, no antenna)
Power Consumption [mW]	**146**	330 (including PA)	80 (Receiver)	43	26	800

customized PCB antenna and a sampling oscilloscope, is shown in Fig. 6. A Polyethylene lens with a focal length of 60mm is placed between the chips to increase the signal power. The total distance between the transmitter and the receiver is 10 cm. Measurement results, including the output spectrum, phase noise, and timing jitter, are shown in Fig. 6. Comparing with the 3.1GHz reference from the signal source, the synchronized signal phase noise has not deteriorated substantially. It should be noted that, at high frequency offsets, phase noise measurement is limited by the spectrum analyzer noise floor due to the low power of the signal, so it becomes flat at -90 dBc/Hz (the actual phase noise is smaller than this value). The receiver generates a 3.1GHz reference clock with a phase noise of -89 dBc/Hz at 100-Hz frequency offset. This also includes the noise contributed by the impulse-radiating chip and the measurement error caused by the low power of the signal. In this measurement, the trigger signal fed to the impulse radiating chip produces a 3.1 GHz signal with 270fs timing jitter and -89 dBc/Hz phase noise at 100 Hz offset. In the two-tone (42 and 48 GHz) test, the receiver generates a 6GHz reference clock with 376 fs timing jitter and -81 dBc/Hz phase noise at 100 Hz frequency offset. The timing jitter of the two-tone experiment is lower than the impulse-based measurement due to the higher power of the radiating source, which makes the jitter measurement more accurate, and results in higher frequency stability. The performance of the chip is compared with the prior art in Table 1.

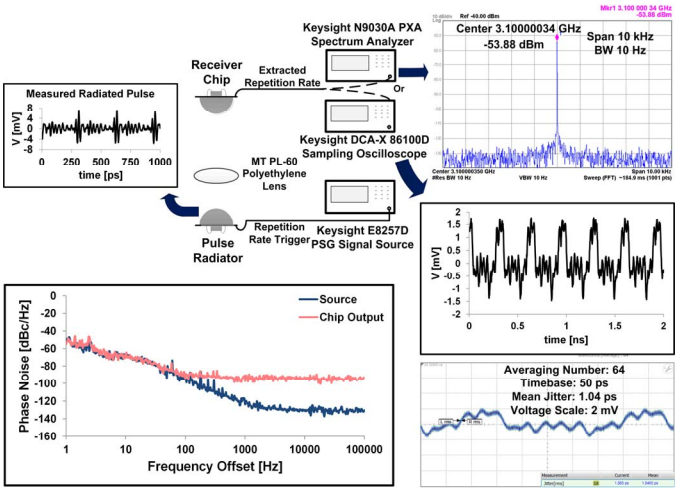

Fig. 6. Test setup for precision time transfer using a picosecond impulse radiator (top left), measured output spectrum of the chip (top right), measured output waveform of the chip (including harmonics and high-frequency couplings) and its timing jitter (bottom right), and the measured phase noise of 3.1GHz carrier at the output compared with the 14-dBm 3.1-GHz source (bottom left).

IV. CONCLUSION

This work introduces a new method for wireless time transfer using ultra-short picosecond pulses. It demonstrates the lowest timing jitter ever achieved in a wireless synchronization system. The chip includes an on-chip antenna, low-noise amplifier, a core nonlinear block, low-pass filter and tunable baseband amplifiers. The chip is fabricated in 0.13µm SiGe BiCMOS process technology. The micrograph of the chip is shown in Fig. 7. To the best of authors' knowledge, this is the first receiver in silicon that can detect sub-8psec electromagnetic pulses.

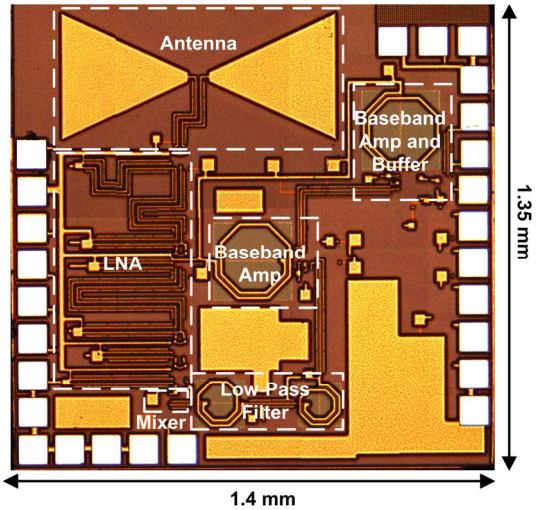

Fig. 7. Chip micrograph of the pulse-based wireless synchronization receiver.

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