Japanese Journal of Applied Physics
Vol. 45, No. 4B, 2006, pp. 3307–3316

Advocating Noise as an Agent for Ultra-Low Energy Computing: Probabilistic Complementary Metal–Oxide–Semiconductor Devices and Their Characteristics

Pinar KORKMAZ[1*], Bilge E. S. AKGUL[1], Krishna V. PALEM[1,2] and Lakshmi N. CHAKRAPANI[1,2]

[1]*Laboratory for Probabilistic Computing from Nanoscale Technologies, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250, U.S.A.*
[2]*College of Computing, Georgia Institute of Technology, Atlanta, GA 30332-0280, U.S.A.*

(Received September 20, 2005; accepted December 21, 2005; published online April 25, 2006)

Noise immunity and low-energy computing have become limiting factors in the semiconductor roadmap as transistor feature sizes shrink. The subject of our study is the probabilistic switch, implemented in the complementary metal–oxide–semiconductor (CMOS) domain, referred to as a probabilistic CMOS (PCMOS) switch, whose behavior is rendered probabilistic by noise. In conducting this study, we are motivated by the possibility of using such probabilistic switches to realize ultra-low energy computing. Based on PCMOS switches realized using 0.5 and 0.25 μm processes, we present detailed analytical models, subsequently verified through HSpice simulations. We consider the thermal noise and power supply noise as our sources for probabilistic behavior. Through one interesting aspect of the study, we characterize the effects of the noise sampling frequency and the output sampling frequency on probabilistic behavior. Finally, we briefly outline the opportunity that such probabilistic switches offer to ultra low-energy computing through the concept of a probabilistic system-on-a-chip (PSoC) architecture (that is based on PCMOS switches); such architectures can achieve significant energy savings and performance improvements at the application level. [DOI: 10.1143/JJAP.45.3307]

KEYWORDS: low-energy computing, noise tolerance, power supply noise, probabilistic CMOS, probabilistic computing, thermal noise

1. Introduction

As complementary metal–oxide–semiconductor (CMOS) devices approach the nano-scale in feature size, the impact of deep submicron noise poses a challenge[1–4] with noise being seen as an impediment to reliable computing. In the 2003 International Technology Roadmap for Semiconductors (ITRS) roadmap,[5] it is stated that increasing noise sensitivity has become an important issue in the design of devices, circuits, and systems due to a reduction in operating voltage by 20% per technology node. On the other hand, an accompanying challenge to CMOS design involves achieving low-energy computation, which has been traditionally addressed by voltage scaling. However, the utility of voltage scaling is decreasing,[6] as reduced voltage levels also reduce noise immunity even further.

In a surprising approach to countering both of these competing needs and rather than treating noise as an impediment, Palem[7,8] outlined a framework for probabilistic switches and computational models based on these switches that treat noise as a resource. These models were used to show that probabilistic algorithms[9] yield low-energy computations. Thus, Palem's work established that well-characterized noise is potentially of value in realizing low-energy computing platforms for probabilistic applications based on probabilistic algorithms.

Palem's work was extended to the CMOS domain by Cheemavalagu *et al.*,[10] wherein a *probabilistic* CMOS (PCMOS) inverter (switch) behavior was characterized in terms of the energy per switching step, noise magnitude, and the probability of correctness p. Subsequently, this work was extended in SSDM 2005[11] to the architecture level, wherein device level benefits of PCMOS switches were outlined in the context of a probabilistic cellular automata[12] application.

*E-mail address: korkmazp@ece.gatech.edu

In this paper, we further develop and detail the device level characterizations of a PCMOS switch originally studied by Cheemavalagu *et al.*[10,13] We consider different types of noise couplings, as well as the effects of the frequency at which noise and the output are sampled on the probabilistic behavior. Further, we also model the probabilistic behavior of a PCMOS switch induced by power supply noise (beyond thermal noise described earlier in refs. 10 and 11). We also consider the effect of short-circuit energy on the probabilistic behavior. Specifically, we analytically model the relationship between the energy per switching E, and the probability of correctness p with different types of noise couplings and validate our models using circuit simulations. We empirically model the effects of the frequencies at which the noise and output are sampled. Our characterization of the effect of short-circuit energy consumption on the probabilistic behavior is also empirical. These details, serving as detailed descriptions and important extension to our work from SSDM 2004,[10] will be the topic of §2 through §6. For completeness, we outline the architecture and application level benefits of PCMOS switches based on our work from SSDM 2005;[11] this outline will be the topic of §7. Finally, we conclude the paper in §8.

2. Basic Concept

For completeness, we introduce the concept of probabilistic switching, and introduce a PCMOS inverter realization of a probabilistic switch (see Palem[8] for precise details).

2.1 Probabilistic switch

A *switch* is a digital device with *one input* and *one output*. The output of the switch is a function f, of the input of the switch. The act of *switching* involves the invocation of the function f, which determines the output of the switch. The act of switching takes some finite amount of time T_s. The

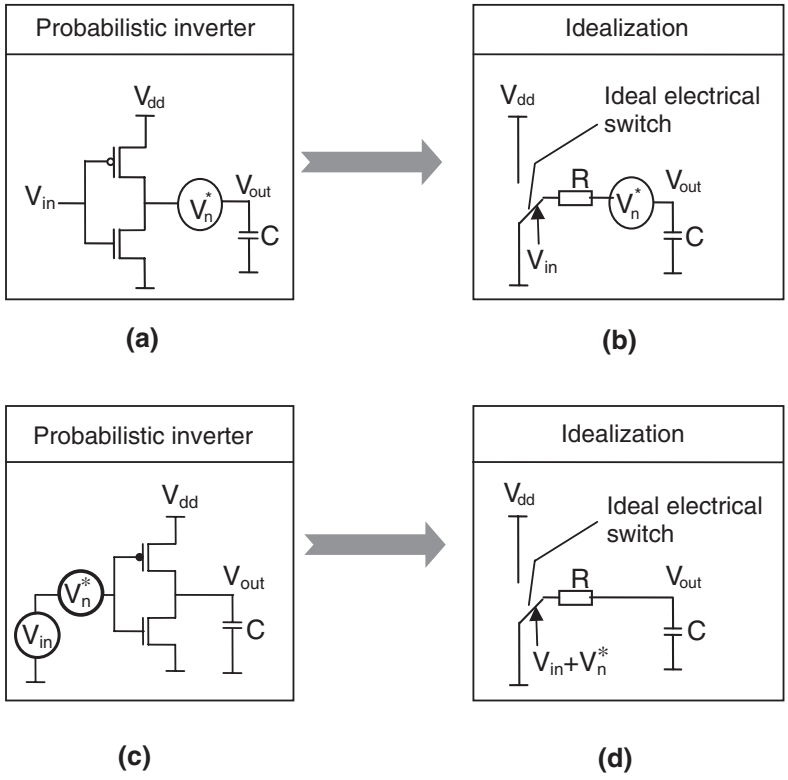

Fig. 1. The idealization of a probabilistic inverter (a,b) when thermal noise is coupled to the output and (c,d) when thermal noise is coupled to the input.

switch and its associated switching can be either deterministic or probabilistic. Let $X(t)$ and $Y(t)$ respectively denote the input and output of a switch where t denotes time. Then, for a *deterministic* switch, $Y(t_2) = f(X(t_1))$, where $f{:}\{0,1\} \rightarrow \{0,1\}$ is a one-input Boolean function, t_2 is the point in time when the switching ends, and t_1 is the point in time when the switching starts. By contrast and in the context of a probabilistic switch, the output $Y(t)$ depends on the probability p as shown in eq. (2.1),

$$Y(t_2) = \begin{cases} f(X(t_1)) & \text{with probability} \quad p\big(1/2 < p < 1\big) \\ \overline{f(X(t_1))} & \text{with probability} \quad 1-p \end{cases} \tag{2.1}$$

where $\overline{f(X)}$ denotes the logical complement of the Boolean function $f(X)$.

2.2 PCMOS inverter realization of a probabilistic switch

Informally, a CMOS inverter is a digital gate that realizes the *complement* function. Switching in this case corresponds to the flow of the switching current through the output capacitance of the inverter. In the context of the switch described in §2.1, for a deterministic inverter, $Y(t_2) = \overline{X(t_1)}$ where X and Y denote the Boolean (henceforth referred to as the *binary* value for convenience) values of the input and the output of the inverter, respectively. The switching time $T_s = (t_2 - t_1)$ is the propagation delay of the inverter.

For a probabilistic inverter, the output to input relationship is described by eq. (2.1). Since in its physical realization the probabilistic switch is a binary device, we digitize the continuous output signal of an inverter using eq. (2.2) below, where the function Y is characterized by the binary value associated with the continuous output signal V_{out}, of the inverter. (The binary input value X can be expressed in a similar manner.)

$$Y(t) = \begin{cases} 1 & \text{if } V_{out}(t) \geq V_m \\ 0 & \text{otherwise} \end{cases} \tag{2.2}$$

In eq. (2.2), V_m denotes the midpoint voltage[14] of the CMOS inverter.

3. Characterization of the Probabilistic Behavior of a CMOS Inverter

In this section, we will first present the analytical model characterizing the probability parameter p of a probabilistic inverter (switch), when thermal noise is coupled to its input, or to its output. Following this, in §3.2, we will model the effect of power supply noise on the probabilistic behavior of a probabilistic inverter. In §3.3, we will establish and discuss the relationship between the energy per switching step E and the probability parameter p, referred to as the E–p relationship of a probabilistic inverter.

3.1 Analytical modeling of the probabilistic inverter with input- and output-coupled thermal noise

For *both* the cases when noise is coupled to the output [Fig. 1(a)] and to the input [Fig. 1(c)] of the inverter—for succinctness and unless otherwise stated, we will refer to a probabilistic inverter as an inverter in the sequel—we use the idealization consisting of an electrical switch in series with a resistor and a capacitor as shown in Figs. 1(b) and 1(d), respectively. We base this idealization of an inverter on the early work of Stein[1] and of Natori and Sano.[2] The resistor R represents the effective resistance of each

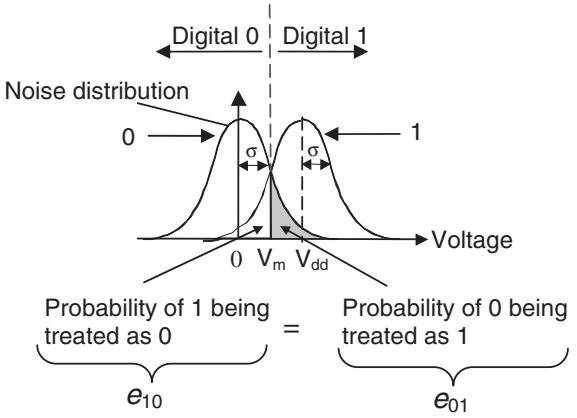

Fig. 2. The digital value 0 (and 1) corresponding to the noisy output (input) voltage of the probabilistic inverter is represented by a Gaussian distribution with a mean value of 0 (or V_{dd}) and a standard deviation σ which is the rms value of the noise—modeled for both the input- as well as the output-coupled cases.

transistor when it is ON,[2] whereas the capacitor C is the output capacitance of the inverter. Recall that the inverter switches at a voltage V_m which corresponds to the midpoint voltage[14] of the inverter.

Following Stein[1] and Pant *et al.*,[15] we consider noise sources to be random processes that are characterized by a Gaussian distribution with a standard deviation σ. Here, the value σ is referred to as the rms value of the noise. Also, in the frequency range of interest, the power spectral density of the noise is a constant, that is all of the frequency harmonics contribute equally to the magnitude.

For simplicity, we model noise as being sampled at the beginning of the switching interval and this sampled value is held constant during the switching interval. In all of our studies, the sampling period of the noise is larger than the propagation delay (T_s) of the inverter and the output voltage (V_{out}) is sampled at the same period as that at which noise is sampled. (Hence, we need not consider the (low-pass) filtering effect of the inverter on the noise.)

The behavior of a noise-induced probabilistic inverter is shown in Fig. 2 and detailed in the caption. As shown there, the digital values of 0 and 1 can be altered by the noise, characterized by a Gaussian distribution so that a value of 0 can, with a sufficiently large noise magnitude, be sampled to be a value of 1 and *vice versa*. The probability of this event is determined by the area under the distribution curve corresponding to the range in question. Thus, in this figure, the probability of the output (input) digital value 0 being treated as 1, and the probability of the output (input) digital value 1 being treated as 0, are respectively, represented by the areas e_{01} and e_{10}; these correspond to the two regions in the intersection of the two noise distributions with a mean value of 0 and V_{dd} respectively. We also note that in this idealization and hence in the figure, $V_m = V_{dd}/2$, which corresponds to the special case when the transistors of the inverter are symmetric.

Given the probabilities of error, e_{01} and e_{10}, the probability of being correct, p, can be expressed as

$$p = 1 - \frac{e_{01} + e_{10}}{2} \tag{3.1}$$

Expressing e_{01} and e_{10} as integrals, evaluating them and substituting the results in eq. (3.1) yield the following relationship between p and V_{dd}.

$$p = \frac{1}{2} + \frac{1}{4}\mathrm{erf}\left(\frac{V_m}{\sqrt{2}\sigma}\right) + \frac{1}{4}\mathrm{erf}\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma}\right) \tag{3.2}$$

In eq. (3.2), erf is the error function defined as $\mathrm{erf}(x) = 2/\sqrt{\pi}\int_0^x e^{-u^2}du$ for a real number x.

3.2 *Analytical modeling of the probabilistic inverter coupled to power supply noise*

Following Pant,[15] power supply noise is characterized by a Gaussian distribution with rms value of σ_p. In this case, we use the idealization illustrated in Fig. 3.

Referring to Fig. 3(a), when $V_{in} = V_{dd}$ and if the power supply noise were not present, the NMOS transistor will be ON and the PMOS transistor will be OFF. This corresponds to a situation where the ideal electrical switch in Fig. 3(b) will be at position 1. Considering the case where $V_{in} = 0$ and if the power supply noise were not present, the PMOS transistor will be ON, and the NMOS transistor will be OFF; therefore the ideal switch will be at position 2. However, due to the power supply noise, the PMOS transistor might be turned ON, even in the case where $V_{in} = V_{dd}$ and might be OFF even though $V_{in} = 0$. Considering the two cases of V_{in} (being either 0 or V_{dd}), we have determined the probability of 1 being interpreted as 0 (e_{10}) and the probability of 0 being interpreted as 1 (e_{01}) and found that the probability of being correct, p, in the case of a probabilistic inverter with power supply noise coupling to be

$$p = \frac{1}{2} + \frac{1}{4}\mathrm{erf}\left(\frac{V_{mp}}{\sqrt{2}\sigma_p}\right) + \frac{1}{8}\mathrm{erf}\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma_p}\right) + \frac{1}{8}\mathrm{erf}\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma_p}\right)\cdot\mathrm{erf}\left(\frac{V_{dd} - |V_{Tp}|}{\sqrt{2}\sigma_p}\right) \tag{3.3}$$

The key steps of the derivations of e_{01} and e_{10}, and V_{mp} parameter of the above equation are summarized below. The details of these derivations can be found in ref. 16.

(1) When $V_{in} = 0$

a. The gate to source voltage of the PMOS transistor is

$$V_{gsp} = -V_{dd} - V_p{}^* \tag{3.4}$$

b. From eq. (3.4), the probability of $|V_{gsp}| < |V_{Tp}|$ (V_{Tp} is the threshold voltage of the PMOS transistor) is

$$Pr\big(|V_{gsp}| < |V_{Tp}|\big) = \frac{1}{2} - \frac{1}{2}\mathrm{erf}\left(\frac{V_{dd} - |V_{Tp}|}{\sqrt{2}\sigma_p}\right) \tag{3.5}$$

c. If $|V_{gsp}| < |V_{Tp}|$, the probability of V_{out} being digital 0 is $\frac{1}{2}$.

d. If $|V_{gsp}| \geq |V_{Tp}|$, the probability of V_{out} being digital 0 is $\frac{1}{2} - \frac{1}{2}\mathrm{erf}(\frac{V_{dd}-V_m}{\sqrt{2}\sigma_p})$.

Hence, the probability of 1 being interpreted as 0 (e_{10}) is

$$e_{10} = Pr(|V_{gsp}| \geq |V_{Tp}|)\cdot\left[\frac{1}{2} - \frac{1}{2}\mathrm{erf}\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma_p}\right)\right] + Pr(|V_{gsp}| < |V_{Tp}|)\cdot\frac{1}{2} \tag{3.6}$$

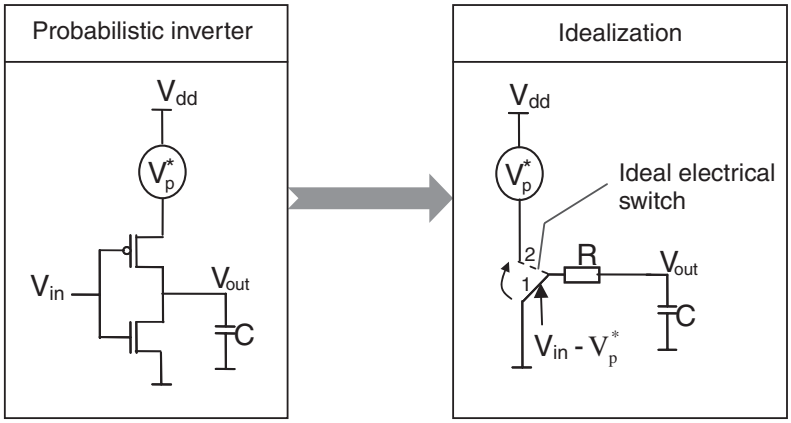

Fig. 3. The approximation to a CMOS inverter coupled with power supply noise.

(2) When $V_{in} = V_{dd}$
   a. V_{gsp} is described by

$$V_{gsp} = V_{dd} - \left(V_{dd} + V_p{}^*\right) = -V_p{}^* \tag{3.7}$$

   b. At the output, an incorrect transition to 1 can occur if $|V_{gsp}| > V_{mp}$ with

$$V_{mp} = \sqrt{\left(\mu_n/\mu_p\right)\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p}V_{dd}\left(\frac{3V_{dd}}{4} - V_{Tn}\right)} + |V_{Tp}| \tag{3.8}$$

   Hence, e_{01} is found to be

$$e_{01} = Pr\left(V_p{}^* > V_{mp}\right) = \frac{1}{2} - \frac{1}{2}\,\mathrm{erf}\left(\frac{V_{mp}}{\sqrt{2}\sigma_p}\right) \tag{3.9}$$

(3) Using eqs. (3.1), (3.6) and (3.9), eq. (3.3) is derived.

3.3 The E–p relationship of a PCMOS inverter

In this section, we will first provide analytical models characterizing the (switching) energy consumed per one switching step, denoted as E, of a PCMOS inverter. Following this, we will depict the relationship between p and E which we refer to as the E–p relationship.

3.3.1 Modeling the energy consumed by a PCMOS inverter per switching step

The main components of dynamic energy consumption of a digital circuit are switching energy consumption (E_{sw}) and short-circuit energy consumption (E_{sc}). In §3.3.2, we will consider the switching energy consumption to characterize the E–p relationship of an inverter. Later, in §5, we present an improved energy model wherein the short-circuit energy consumption is also included.

3.3.2 Deriving the E–p relationship for a PCMOS inverter

We model the switching energy consumption to be

$$E_{sw} = \frac{1}{2}CV_{dd}^2 \tag{3.10}$$

where the energy consumed is that used to charge or discharge a capacitive load C of the RC circuit idealization of an inverter shown in Figs. 1 and 3.

Recall from eqs. (3.2) and (3.3) that p is a function of V_{dd}. We denote this function by h_i, where i is an integer associated with the type of coupling. Since, we have considered three cases of coupling, $i \in \{1, 2, 3\}$, where input-coupled thermal noise, output-coupled thermal noise and power supply noise are associated with indices $i = 1$, 2 and 3 respectively. Thus, for input coupled noise serving as a basis for our probabilistic inverter, $p \equiv h_1(V_{dd})$, and from eq. (3.2)

$$h_1(V_{dd}) = \frac{1}{2} + \frac{1}{4}\,\mathrm{erf}\left(\frac{V_m}{\sqrt{2}\sigma}\right) + \frac{1}{4}\,\mathrm{erf}\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma}\right) \tag{3.11}$$

Equivalently, $V_{dd} = h_1^{-1}(p)$ where $h_i^{-1}(x)$ denotes the inverse of the function $h_i(x)$ for a real valued x. With the power supply noise coupling, on the other hand, $h_3(V_{dd})$ is

$$h_3(V_{dd}) = \frac{1}{2} + \frac{1}{4}\,\mathrm{erf}\left(\frac{V_{mp}}{\sqrt{2}\sigma_p}\right) + \frac{1}{8}\,\mathrm{erf}\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma_p}\right) + \frac{1}{8}\,\mathrm{erf}\left(\frac{V_{dd} - V_m}{\sqrt{2}\sigma_p}\right)\cdot\mathrm{erf}\left(\frac{V_{dd} - |V_{Tp}|}{\sqrt{2}\sigma_p}\right) \tag{3.12}$$

From eq. (3.10) by substituting $h_i^{-1}(p)$ for V_{dd}, the generalized E–p relationship which is our analytical model is

$$E = \frac{1}{2}C\left[h_i^{-1}(p)\right]^2 \tag{3.13}$$

For example, if the transistors of the inverter are symmetric (having identical threshold voltages ($|V_{Tp}| = V_{Tn}$) and satisfying the condition $(\mu_n/\mu_p) = (W/L)_p/(W/L)_n$),[14] and considering an inverter rendered probabilistic by thermal noise coupled to the input or the output of this inverter, the analytical model characterizing the E–p relationship can be specialized to yield

$$E = 4C\sigma^2\left[\mathrm{inverf}\left(2p - 1\right)\right]^2 \tag{3.14}$$

where inverf is the inverse of the error function.[17]

The expression in eq. (3.14) shows that E, the energy to produce a probabilistic bit, grows with p and the order of this growth dominates an exponential (see ref. 18). We also

Table I. Simulation parameters for inverters in AMIS 0.5 μm and TSMC 0.25 μm processes.

Technology		AMIS 0.5 μm	TSMC 0.25 μm
Inverter fan-out		4	4
Load capacitance (fF)		60	28
Nominal V_{dd} (V)		5	2.5
Transistor size	$(W/L)_{pmos}$	15 u/0.6 u	2 u/0.3 u
	$(W/L)_{nmos}$	6 u/0.6 u	0.8 u/0.3 u
V_{dd} (V)		0.8–5	0.5–2.5
σ (V)		0.2–0.8	0.2–0.8
σ_p (V)		0.2–0.8	0.2–0.8
Input rise- and fall-times (ns)		0.2	0.2

see from eq. (3.14) that the energy consumed to produce a bit increases quadratically with noise rms value σ, for a fixed probability value p. A detailed statement of these two trends can be found in a companion paper by Korkmaz and Palem.[18)]

4. Validation of Analytical Models

To validate our analytical model of a probabilistic inverter [eq. (3.13) from §3.3.2] we performed circuit simulations in HSpice using models of inverters realized using AMI Semiconductor (AMIS) 0.5 μm and Taiwan Semiconductor Manufacturing Company (TSMC) 0.25 μm processes. The simulation parameters are summarized in Table I. As seen in the table, these parameters include the supply voltage (V_{dd}), the rms value of the thermal noise (σ), as well as rms value of the power supply noise (σ_p). The load capacitance value (C) corresponds to the capacitive load due to a fanout of four (which is the typical value of load used especially for delay calculations[19,20)]), leading to values of 60 and 28 fF for 0.5 and 0.25 μm processes, respectively. We will now detail the simulation results based on the 0.25 μm process. The results for an inverter realized using the 0.5 μm process show similar trends.

4.1 Modeling of noise in circuit simulations

In our simulations, noise is injected into the HSpice "netlists" in the form of a PWL (piecewise linear) voltage source. The data points of the PWL source are derived from a Gaussian distribution of random numbers generated by Matlab. We show a sketch of an example noise pulse in Fig. 4. As shown there, t_{nr} and t_{nf} denote the rise and fall times of the noise pulse, and they are identical, whereas t_{nc} denotes the length of the time during which the noise voltage is held at a constant value. In addition, t_{sn} denotes the sampling period of the noise, and is equal to the sum of the values t_{nf} (or t_{nr}) and t_{nc}.

In §3.1, we stated that noise is sampled at the beginning of the switching step, and that it is held constant during switching, and that the sampling period of the noise is larger than the switching time (T_s) of the inverter. We refer to this process of sampling and holding the noise voltage, as the process of *latching* the noise and such a noise source as *latched* noise. Thus, we first consider the case where noise is latched since our analytical model is developed based on this case. In general, on the other hand, for a noise source in transient response circuit simulations,[21)] t_{nc} is identical to zero (Fig. 4). We refer to this case of injecting noise as *not-latching* the noise and such a noise source as *non-latched* noise. Subsequently, in §6, we will consider the case that noise is not latched, and we will illustrate its impact on the probabilistic behavior of the inverter. In addition, in the current section, V_{out} is sampled with the same sampling period as that of the noise.

4.2 Measurement of the energy E and the probability p during circuit simulations

The energy per switching step E is determined by measuring the total current drawn from the voltage supply node of the inverter during the time that the inverter switches, where the switching is induced by a pulse source applied to its input. For completeness, the last row of Table I shows the value of the rise and fall times of the input pulse. We note that we only measure the energy consumed by a CMOS inverter while its output changes (switches) from 0 to V_{dd} or *vice versa*.

The value of p is measured to be the ratio of the number of the correct simulation points measured at the output of the inverter to the ratio of the total number of simulation points.

We will now compare the analytical and simulation results for the E–p relationship of a probabilistic inverter that is coupled with thermal noise at its input or its output. Following this, we compare the analytical and simulation results for the E–p relationship of a PCMOS inverter coupled with power supply noise.

4.3 The E–p relationship for a PCMOS inverter coupled to thermal noise

In Fig. 5, we depict the E–p relationship of PCMOS inverters realized using 0.25 and 0.5 μm processes, both

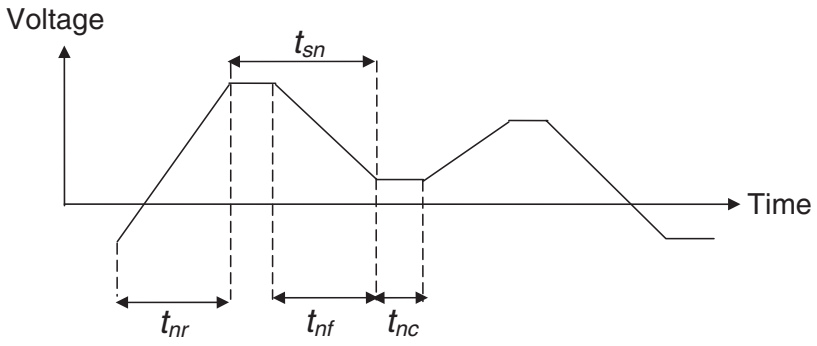

Fig. 4. The noise pulse and its rise and fall times.

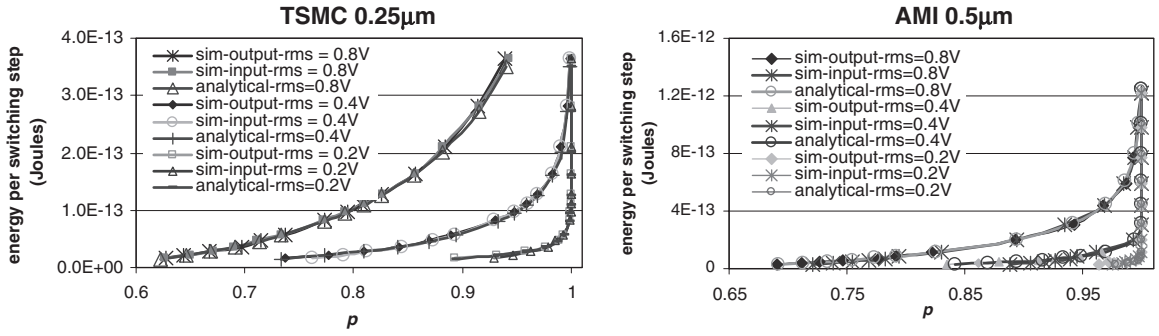

Fig. 5. The E–p relationship for inverters coupled to thermal noise at their inputs or outputs.

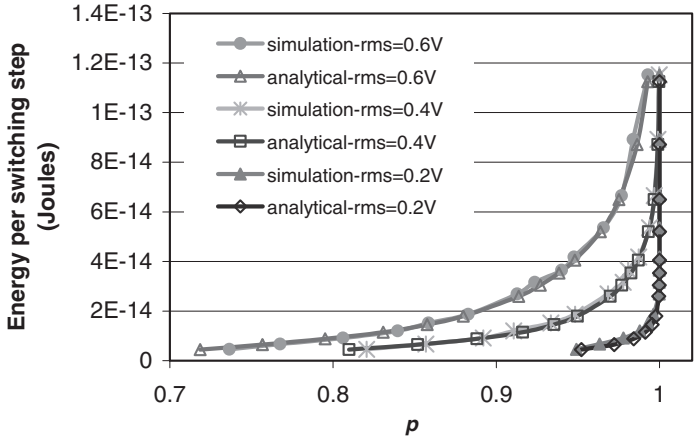

Fig. 6. The E–p relationship with power supply noise coupling.

coupled to thermal noise at their outputs or inputs. The two parameters that we vary are the noise rms value σ and the operating supply voltage V_{dd}. In particular, for each value of σ, we compare values of the parameter p determined at different values of V_{dd} using the analytical model [eq. (3.2)] with those determined using circuit simulations. In Fig. 5, sim-output denotes the simulation results in the case of output-coupled thermal noise and sim-input denotes the simulation results in the case of input-coupled thermal noise. Recall that we estimate the energy consumed per switching step of the inverter analytically using eq. (3.10). As shown in Fig. 5, the difference between the results of analytical model and simulations is negligible. The maximum deviation between the analytically estimated and the simulated results is 3.92%, a value that can not be visually noticed. To reiterate, given a fixed amount of available noise, the energy needed to produce a single bit grows with p, and the order of this growth dominates an exponential. Furthermore, for a fixed probability value of p, the energy consumed to produce a bit increases quadratically with noise rms.

4.4 The E–p relationship for a PCMOS inverter coupled to power supply noise

The E–p relationship of an inverter coupled to power supply noise is shown in Fig. 6. Again we vary the supply voltage of the inverter and the rms value of the power supply noise coupled to the inverter. The trends relating E to p, and to the noise rms value are similar to those observed in cases of the input- and output-coupled thermal noise discussed before. As seen in Fig. 6, the difference between the analytical results and the simulation results is negligible and is a maximum of 3.8%.

4.5 Comparing thermal and power supply noise couplings

In Fig. 7, we compare the E–p relationship of an inverter coupled to thermal noise with the one coupled to power supply noise. In the legend of this figure, thermal-rms denotes the rms value of thermal noise, whereas ps-rms denotes the rms value of the power supply noise. As seen from the figure, at a fixed value of E, output-coupled thermal noise is more effective and induces a lower value of p when compared to the power supply noise of the same rms value. (See points A and B in Fig. 7 for example, both of which correspond to an rms value of 0.6 V and are respectively associated with thermal and power supply noise. Similarly, points marked C and D correspond to an rms value of 0.4 V.) Thus, output-coupled thermal noise is more effective in realizing a specific value of p, since the required value of noise rms in the case of the output-coupled thermal noise is lower than the corresponding value for power supply noise. This is due to the fact that power supply noise induces less errors when $V_{in} = V_{dd}$ (see ref. 16); namely when the switch (in Fig. 3) is at position 1 for the most part, the noise source on the supply node will be isolated.

5. An Improved Energy Model Accounting for Short-Circuit Energy

In §4, we have observed a negligible difference between the analytically estimated E–p relationship and the E–p relationship found through HSpice simulations. In these

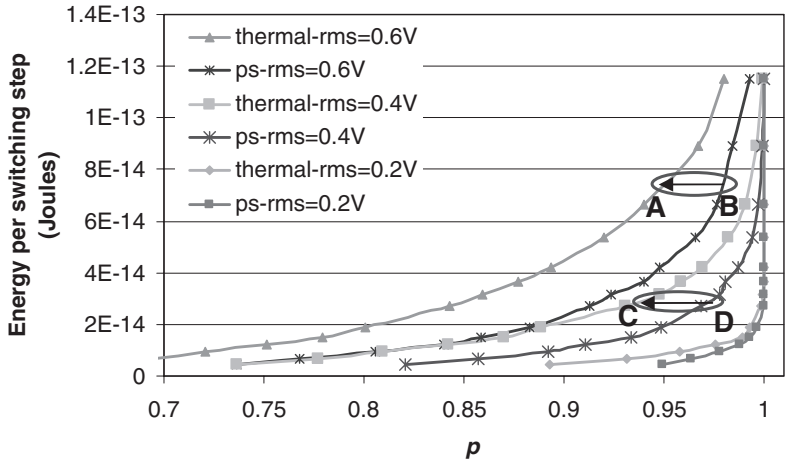

Fig. 7. Comparison of the E–p relationships in the instances of power supply noise coupling and output-coupled thermal noise.

Table II. Simulation parameters for an inverter driving a high capacitive load.

Technology		TSMC 0.25 µm
Inverter fan-out		7
Load capacitance (fF)		130
Nominal V_{dd} (V)		2.5
Transistor size	$(W/L)_{pmos}$	6.72 u/0.24 u
	$(W/L)_{nmos}$	3.36 u/0.24 u
V_{dd} (V)		1.5–2.5
σ (V)		0.2–0.8
σ_p (V)		0.2–0.8
Input rise- and fall-times (ns)		2

models and simulations, the physical (transistor) parameters yield very low short-circuit energy. In the current section, we consider a different scenario wherein the short-circuit energy consumption of the inverter is significant, and hence, the analytical model based energy estimates from §3 deviate from the simulation results.

In Table II, we show the simulation parameters of an inverter with larger transistors and a larger capacitive load than those considered before. Further, the rise and fall time of the input signal is higher than the value considered in §4. In our study, the load capacitance, which is 130 fF (as shown in Table II) corresponds to the sum of the drain capacitances of the inverter transistors, and the input capacitance of an output driver connected to a chip pin. In Fig. 8(a), we show the E–p relationship of the inverter (with the parameters shown in Table II) in the case of input-coupled thermal noise; similar trends and derivations are observed with other noise couplings as well. As seen in Fig. 8(a), there is a significant difference between the simulation and analytical results, to be contrasted with the lack of such deviation shown in Fig. 5 when the capacitive load C, the transistor sizes, and the rise and fall time of the input pulse are smaller. The significant deviation shown in Fig. 8(a) is due to the fact that the analytical model discussed so far does not account for the short-circuit energy component which is a part of the HSpice based estimates.

We have developed a short-circuit energy model following Bisdounis and Koufopavlou.[22] In our model, we explicitly use the alpha-power (α-power) law MOSFET model of Nose and Sakurai.[23] Applying our model to derive short-circuit energy (E_{sc}), the total energy consumed by a CMOS inverter per switching will be

$$E = E_{sc} + E_{sw} \tag{5.1}$$

where E_{sw} is the switching energy estimated in earlier sections.

Using eq. (5.1) to estimate the energy consumption of the probabilistic inverter (with the parameters shown in Table II), the resulting E–p relationship is shown in Fig. 8(b). As seen in the figure, the analytically obtained E–p relationship matches extremely well with the E–p relationship obtained through simulations. Specifically, the maximum deviation between the analytically modeled and simulated values goes (down) to 2.77% when short-circuit energy is accounted [in Fig. 8(b)] from a value of 49.15% when short-circuit energy is not accounted [in Fig. 8(a)]. In this paper, we limit our discussion to this empirical observation; details of the analytical model including the short-circuit energy consumed during switching can be found in ref. 16 and will be published in the future.

6. The Impacts of Output Sampling Frequency and Noise Sampling Frequency on the Probabilistic Behavior of an Inverter

In §3, we postulated the sampling period of the noise to be larger than the propagation delay of the inverter. We also postulated that the output voltage of the inverter (V_{out}) is sampled at the same rate as the noise. In the sequel, we refer to the sampling period of the noise as t_{sn}, and the sampling period of V_{out} as t_{so}. Hence, the output sampling frequency is $1/t_{so}$ and the noise sampling frequency is $1/t_{sn}$. However, in a realistic scenario, the noise sampling period may not be larger than the period of switching. Similarly, due to a variation in the period, the output sampling frequency may not be equal to the noise sampling frequency. To comprehensively study the effects of these two frequency (or time period) parameters on the probabilistic behavior of a CMOS inverter, in §6.1 below, we will empirically characterize the effect of varying output sampling frequency and in §6.2, that of varying the noise sampling frequency.

Recall that, in §4, we discussed the characteristic noise

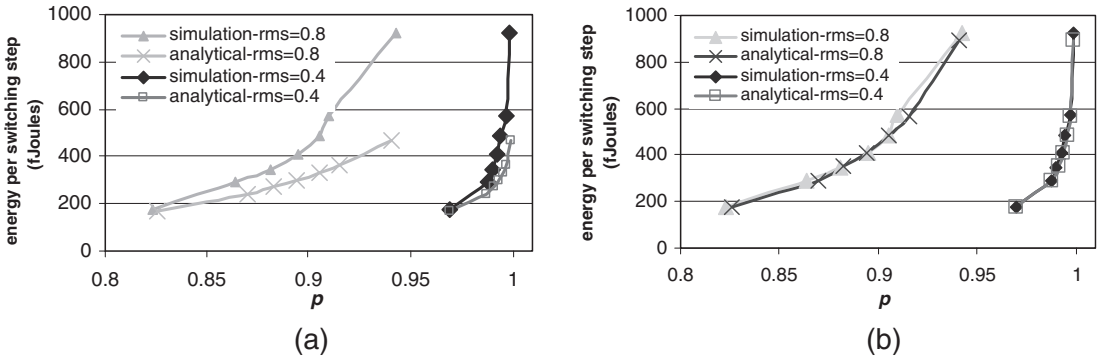

Fig. 8. The E–p relationship of the CMOS inverter with the parameters shown in Table II where the analytical model (a) does not include the short-circuit energy (b) includes the short-circuit energy component.

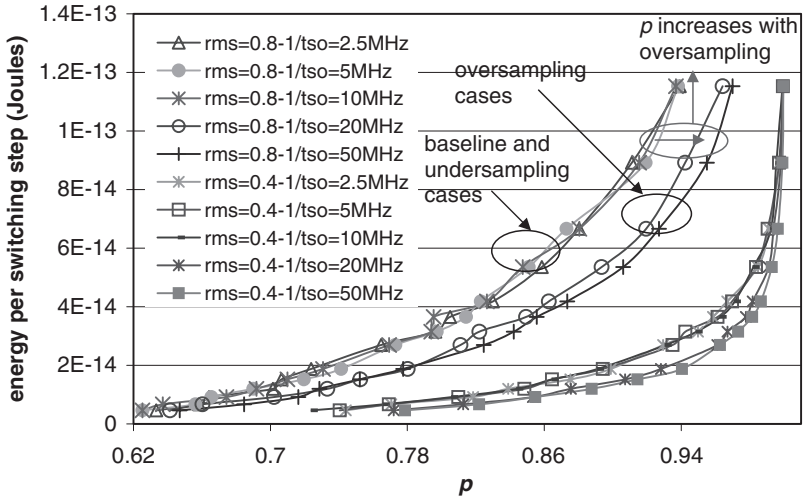

Fig. 9. The impact of t_{so} on the E–p relationship.

pulse (see Fig. 4) that is used in circuit simulations and we introduced two types of noise sampling: (1) when noise is latched, and (2) when noise is non-latched. Specifically, our results in §4 were based on the case where noise is latched. In the current section, we will complete this study by considering the case of non-latched noise, which is more realistic.

6.1 *The impact of output sampling frequency on the E–p relationship*

To investigate the effects of varying the output sampling frequency, we consider oversampling (wherein the voltage V_{out} of the inverter is sampled more frequently than the output-coupled thermal noise) and undersampling (wherein the voltage V_{out} of the inverter is sampled less frequently than the output-coupled thermal noise). Since similar trends are observed in case of the other types of noise couplings, we limit ourselves to a discussion of the effects of the output-coupled noise. In this section, we consider a CMOS inverter with the parameters shown in Table I for our HSpice simulations.

In Fig. 9, we show the impact of oversampling and undersampling on the E–p relationship in the case of output-coupled non-latched noise. Note that the case when the output sampling frequency, $1/t_{so}$, has a value of 10 MHz—and is then equal to the sampling frequency of noise—is referred to as the baseline. The output sampling frequency ($1/t_{so}$) values of 5 and 2.5 MHz correspond to the case when the output is undersampled. Similarly, the output sampling frequency values of 20 and 50 MHz correspond to the case where the output is oversampled. As in the previous section, our development will be limited to an empirical discussion. Mathematical models and derivations can be found in the work of Korkmaz *et al.*[16] and will be subject of a future publication.

In case of oversampling, since the effective value of noise rms decreases (see ref. 16), the p value is increased at a fixed value of the switching energy E; this trend is shown in Fig. 9. Also seen in Fig. 9, oversampling beyond $2/t_{sn}$ ($1/t_{so} > 2/t_{sn}$) has negligible impact on the value of p, especially at small values of noise rms.

In case of undersampling, however, the effective rms value of noise remains the same (provided that the number of output samples is large enough to preserve the original Gaussian distribution), and hence, p is not affected. Therefore, we expect undersampling not to affect on the E–p relationship, which is also seen from Fig. 9.

6.2 *The impact of noise sampling frequency on the E–p relationship*

In this section, we investigate the impact of the noise sampling frequency on the E–p relationship for an inverter

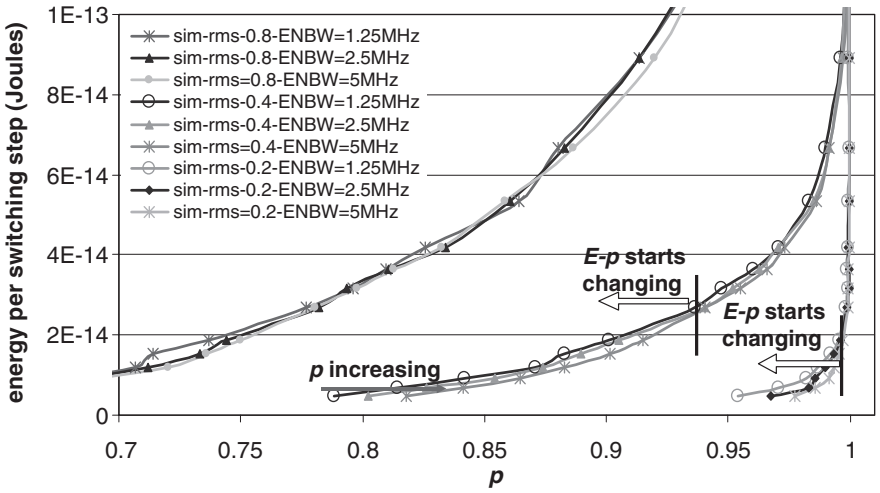

Fig. 10. The E–p relationship for different values of ENBW.

with input-coupled thermal noise. We only focus on the case of input coupling rather than the cases of output coupling or power supply noise coupling due to the following reasons. First, we have observed that the noise sampling frequency has negligible effect on the probabilistic behavior for the output-coupled noise. Second, our study of the effect of the noise sampling frequency for the case of power supply noise has yielded results similar to those described below in the case of input-coupled thermal noise; thus these results are not included in this paper for brevity.

In our circuit simulations, we now consider the case of non-latched noise. Given that noise is sampled at the rate $1/t_{sn}$, the maximum frequency component of the noise should be smaller than $1/2t_{sn}$ (from Nyquist's criterion). In what follows, we will refer to $1/2t_{sn}$ as the equivalent noise bandwidth, denoted as ENBW. In the results shown below, the noise and the output are sampled at the same frequency ($S = 1/t_{sn} = 1/t_{so}$).

In Fig. 10, we show the E–p relationship of the PCMOS inverter (with the parameters from Table I) for different values of ENBW and for different values of noise rms. Again and in keeping with the empirical style of this section, the E–p relationships for different values of ENBW are obtained through HSpice simulations. As seen from Fig. 10, the value of ENBW has negligible impact on the E–p relationship with a noise rms value of 0.8 V. However, for the noise rms values of 0.4 and 0.2 V, we observe that the E–p relationship is affected by the value of ENBW once a specific value of p is reached. For example, when the rms value of noise is 0.4 V, we observe that, for $p \leq 0.94$, p increases as the value of ENBW increases, for a fixed value of switching energy E. We observe that this trend is due to the higher propagation delay of the inverter at small values of p and hence that of the voltage V_{dd}. For the same reason, we note that the trend is more prominent at small values of noise rms since the input-coupled noise with a small rms value implies a smaller input voltage magnitude increasing the propagation delay of the inverter by slowing its switching time.

7. Application Impact

So far, we have presented characterization of the PCMOS switch behavior. In this section, we show the utility of such PCMOS switches and quantify the energy savings possible through using PCMOS technology in implementing one probabilistic application. We note that probabilistic methods[9] have a wide range of applications in different areas, such as pattern recognition, encryption, classification, and optimization. We wish to emphasize that the description in this section is merely meant to highlight the value and utility of PCMOS technology to probabilistic applications, and is not the subject of this paper. Rather, the architectural and application oriented benefits of PCMOS technology can be found in a companion publication due to Chakrapani *et al.*[24]

As we will sketch below, PCMOS devices can be used to build probabilistic system-on-a-chip (PSoC) architectures. The application- and architecture-level savings are quantified using the product of the energy consumed (measured in Joules) and the performance (measured in seconds), denoted *energy* × *performance*. We present an outline of the low-energy computing PSoC architectures based on PCMOS, and the accompanying benefits in the context of the probabilistic cellular automata (PCA) application.[12]

7.1 Probabilistic system-on-a-chip (PSoC) architectures

To realize energy efficient embedded computing platforms, we have developed a methodology for using PCMOS. As shown in Fig. 11 (and discussed in detail by Chakrapani *et al.*[24]), a PSoC architecture is comprised of a host processor and a co-processor where the host processor is used to compute most of the control-intensive deterministic components of an application, whereas the co-processor realized using PCMOS can be viewed as an energy-performance accelerator that executes the probabilistic content of the application.

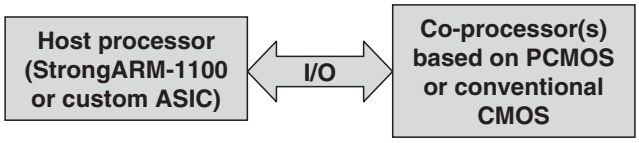

Fig. 11. A probabilistic system-on-a-chip architecture following Chakrapani *et al.*[24]

Table III. EPP Gain of PCMOS over CMOS and over conventional software based implementation running on StrongARM SA-1100 processor to execute the primitive probabilistic operation of PCA.

Algorithm	Application	Primitive operation	Gain	
			over CMOS	over software
PCA	String classification	Evaluating the probabilistic transition function	7.74×10^2	4.17×10^4

We compared the gain of a PSoC based implementation over a functionally equivalent SoC realized using conventional CMOS technology—both the PCMOS and CMOS designs are realized using a 0.25 μm TSMC process. The gain of the PSoC over SoC is defined as the ratio of the energy-performance product (EPP) of the SoC implementation to the EPP of PSoC implementation: $Gain = \mathrm{EPP}_{\mathrm{SoC}}/\mathrm{EPP}_{\mathrm{PSoC}}$. The gain of the PSoC design over the SoC design is a factor of 774 in the context of a core primitive probabilistic operation of the PCA application (see Table III), whereas it is a factor of 561 (not shown in the table) in the context of the overall execution of the string classification application solved using a PCA (see ref. 24 for details).

8. Concluding Remarks

In this paper, we have presented the results of a study of the energy-probability or E–p relationship of a probabilistic inverter. We have considered different couplings of noise, which include the input-, and output-coupled thermal noise, and power supply noise coupling. The main contribution involved the development of analytical models whose quality was validated by simulation results for all three instances of noise coupling.

Throughout, we have considered "controllable" noise sources, wherein the spectral distribution and the sampling frequency of the noise are known *a priori*. We have empirically determined that sampling frequency of the noise is also critical in determining the probability parameter p associated with an inverter. Furthermore, the frequency at which the output of a probabilistic inverter is sampled has also been shown to affect the probability parameter p.

Our work provides analytical models and insights to the circuit designers who might wish to exploit noise in realizing probabilistic designs yielding PSoC architectures—such architectures are the subject of a companion paper.[24] Thus, using our analytical models, one can design circuits and ultra energy-performance efficient PSoC architectures as outlined in §7.

Acknowledgements

This work is supported in part by DARPA under seedling #F30602-02-2-0124, by the DARPA ACIP program under contract #FA8650-04-C-7126 through a subcontract from USC-ISI, and by an award from Intel Corporation.

1) K.-U. Stein: IEEE J. Solid State Circuits **12** (1977) 527.
2) K. Natori and N. Sano: J. Appl. Phys. **83** (1998) 5019.
3) L. Kish: Phys. Lett. A **305** (2002) 144.
4) R. Hegde and N. R. Shanbhag: IEEE Trans. VLSI Syst. **8** (2000) 379.
5) ITRS 2003 Edition. http://public.itrs.net/Files/2003ITRS/Home2003.htm
6) R. Gonzalez, B. M. Gordon and M. Horowitz: IEEE J. Solid State Circuits **32** (1997) 1210.
7) K. V. Palem: Proc. Int. Symp. Verification (Theory and Practice), 2003, p. 524.
8) K. V. Palem: IEEE Trans. Comput. **54** (2005) 1123.
9) R. Motwani and P. Raghavan: *Randomized Algorithms* (Cambridge University Press, Cambridge, 1995).
10) S. Cheemalavagu, P. Korkmaz and K. V. Palem: Ext. Abstr. Int. Conf. Solid State Devices and Materials, 2004, p. 402.
11) K. V. Palem, L. N. Chakrapani, B. E. S. Akgul and P. Korkmaz: Ext. Abstr. Int. Conf. Solid State Devices and Materials, 2005, p. 678.
12) H. Fuks: Phys. Rev. E **66** (2002).
13) S. Cheemalavagu, P. Korkmaz, K. V. Palem, B. E. S. Akgul and L. N. Chakrapani: Proc. IFIP Int. Conf. Very Large Scale Integration, 2005, p. 452.
14) J. P. Uyemura: *CMOS Logic Circuit Design* (Kluwer Academic, Boston, 1999).
15) S. Pant, D. Blaauw, V. Zolotov, S. Sundareswaran and R. Panda: Proc. Design Automation Conf., 2004, p. 171.
16) P. Korkmaz, B. E. S. Akgul and K. V. Palem: Tech. Rep. CREST-TR-05-08-01. Available at http://www.crest.gatech.edu/palempbitscurrent/.
17) A. J. Strecok: Math. Comput. **22** (1968) 144.
18) P. Korkmaz and K. V. Palem: Tech. Rep. CREST-TR-06-02-01. Available at http://www.crest.gatech.edu/palempbitscurrent/.
19) R. Ho, K. Mai, H. Kapadia and M. Horowitz: Proc. Int. Conf. Computer Aided Design, 1999, p. 425.
20) M. S. Hrishikesh, N. P. Jouppi, K. I. Farkas, D. Burger, S. W. Keckler and P. Shivakumar: Proc. Annu. Int. Symp. Computer Architecture, 2002, 14.
21) J. A. Connelly and P. Choi: *Macromodeling with SPICE* (Prentice-Hall, Englewood Cliffs, 1992).
22) L. Bisdounis and O. Koufopavlou: IEEE Trans. Circuits Syst. **47** (2000) 1350.
23) K. Nose and T. Sakurai: IEEE Trans. Comput.-Aided Des. IC Syst. **19** (2000) 1023.
24) L. N. Chakrapani, B. E. S. Akgul, S. Cheemalavagu, P. Korkmaz, K. V. Palem and B. Seshasayee: Proc. Design Automation and Test in Europe (DATE), 2006, p. 1110.