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VLSI Architecture for High Definition Digital Cinema Playback System

by

Guohui Wang

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Approved, Thesis Committee:

Yiqiang Chen, Chair
Associate Professor of Institute of
Computing Technology, CAS

Zhensong Wang
Professor of Institute of Computing
Technology, CAS

Lisheng Zhang
Associate Professor of Institute of
Computing Technology, CAS

Ping Yao
Associate Professor of Institute of
Computing Technology, CAS

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ABSTRACT

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Guohui Wang

Directed by Professor Zhensong Wang

This paper presents a high performance VLSI architecture for the playback system of high definition digital cinema server that complies with Digital Cinema Initiatives (DCI) Specification. This architecture is VLSI friendly so that it can be easily implemented using FPGA and SOC video codec chips. Several key techniques of this architecture are discussed.

This paper introduces the requirement of DCI Specification and then gives an overview of the architecture for the playback system for the digital cinema server. In order to process the video stream with high bitrate and complex stream constitution in the real-time, a configurable high speed buffer is proposed, which uses ping-pong structure memory and dynamic buffer management method. It can be configured to support both 2k and 4K high definition digital movies.

In addition, since the DCI Specification has a strict requirement on the Quality of Service (QoS). When playing a high definition movie, the synchronization between the video track and the audio track becomes quite significant. Taking the characteristic of data structure used for digital cinema into account, a new approach to ensure the synchronization is provided, which is based on the high speed buffer and the frame look-up table. Moreover, this approach can be easily implemented in FPGA.

Furthermore, this paper introduces the architecture of the system information feedback system, which could feedback information required by the central control software running on the server. Employing a hierarchical design, this system is divided into three parts: hardware-software interface module, information gathering and coding module, and information feedback controller. This information feedback system can be used to convey regular run-time information to the server or to diagnose problems when the digital cinema server exceptionally breaks down.

The digital cinema server described in this paper has been successfully implemented with FPGA and SOC chips, which fully complies with the DCI Specification and supports the JPEG2000 digital cinema content with the bitrate up to 350Mbps. The video and audio track can also be precisely synchronized during the playback.

Keywords: DCI; Digital Cinema Server; Playback System; VLSI Architecture;