

ELEC 326

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1 Physical properties of gates

Over the next 1–2 lectures, we will discuss some of the physical characteristics of integrated circuits. It reviews and expands on material covered in Elec 220 and introduces concepts from ELEC 261/305 as well. We will

- review the structure of MOS transistors,
- develop a very simple structural model for gates that demonstrates how they work,
- introduce some special types of gates, including transmission, tri-state, and open collector gates,
- discuss some of the differences between real and ideal gates,
- discuss some of the physical properties of gates,
- understand how timing, voltage, and current properties of real gates are described,
- look at analysis and synthesis of gate networks, and
- conclude with an introduction to Verilog and its use in specifying gate network behavior.

Use this list as a starting point to explore chapters 2, 3, and 4 in the textbook.

2 MOSFET transistors

Metal-oxide-semiconductor field effect transistors (MOSFETs) are the transistors most widely used in integrated circuits today. The name is due to:

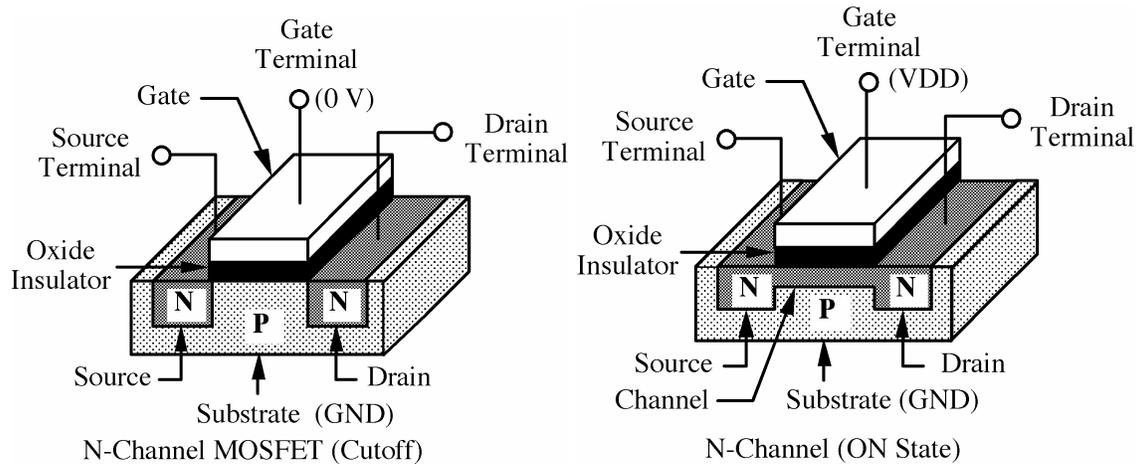
- the device structure – a sandwich of a metal conductor, an oxide insulator, and a semiconductor substrate and
- the way it works – an electric field controls the flow of current through the device.

Although early MOSFET transistors used metal for the first layer, current ones use a polysilicon material (a conductor with somewhat more resistance than a conductor), which is easier to fabricate

2.1 n-Channel MOSFET transistors

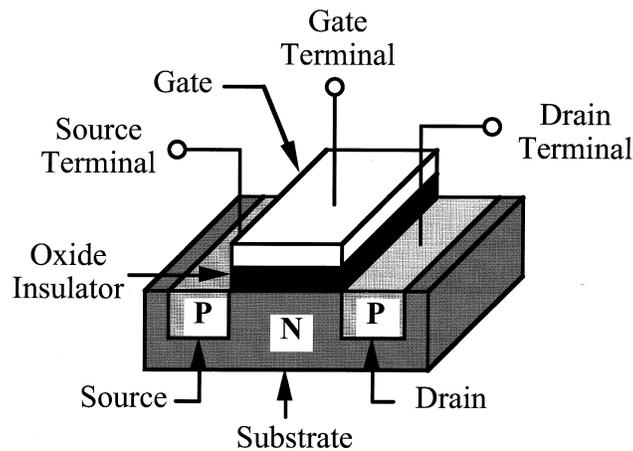
- With no voltage between the gate terminal and the substrate, there are two junctions between the two n regions and the p region.
- This acts like two oppositely connected diodes, and no current can flow between the source and the drain.
- Application of a positive voltage between the gate terminal and the substrate creates an electric field that drives holes out of the region under the gate, creating a channel of n-type material that connects the source and drain terminals.

- Current is due to electron movement
- Tap analogy
- Sub-threshold, linear, and saturation regions of operation
- Standard notation that you will encounter includes supply voltage V_{DD} , gate-to-source voltage V_{GS} , drain-to-source voltage V_{DS} , and threshold voltage $V_{T,n}$

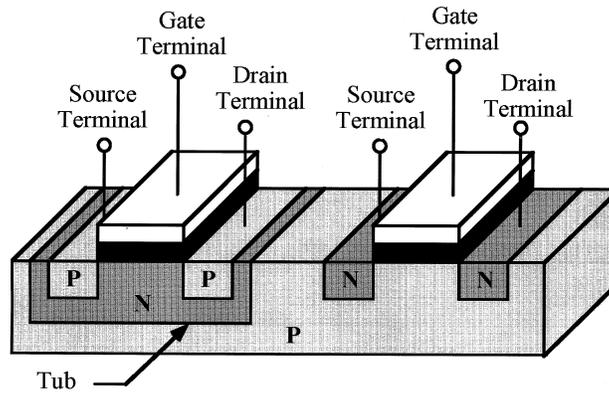


2.2 p-Channel MOSFET transistors

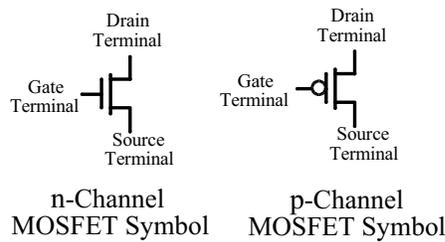
- The p and n regions are reversed from the n-Channel device.
- Application of a voltage on the gate terminal that is negative relative to the substrate creates a p channel beneath the gate and charge flow is due to hole movement.



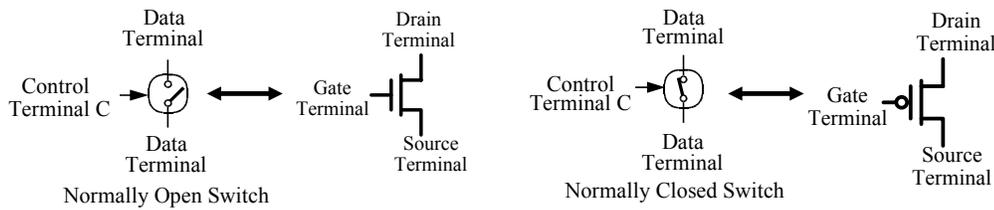
2.3 Complementary MOSFETS (CMOS)



- n-channel and p-channel transistors can be fabricated on the same substrate as shown above
- The following symbols are used to represent MOSFET transistors in circuit diagrams:



- The ideal normally closed switches that we will encounter soon are models for the MOSFET transistors



3 Gates

A *gate* can be thought of as a simple electronic circuit (a system) that realizes a logical operation.

- The direction of information flow is from the input terminals to the output terminal.
- The number of input and output terminals is finite and they carry binary-valued signals (i.e., 0 and 1). More on this when we discuss noise margins in digital circuits.
- The transformation of input signals to output signals can be modeled as a logical operation.

3.1 Truth tables

- Since there is a finite number of input signal combinations, we can represent the behavior of a gate by simply listing all of its possible input configurations and the corresponding output signal. Such a list is called a truth table.

- The use of the symbols H/1 and L/0 usually correlates with the high and low voltages and is the positive logic convention that we will use for the rest of this course.
- Recall the standard gates that you encountered in 220, their symbols, and their truth tables.
- Gates with more than 3 inputs:
 - And gates: The output is 1 if and only if ... ?
 - Or gates: The output is 1 if and only if ... ?
 - Nand gates: The output is 0 if and only if ... ?
 - Nor gates: The output is 0 if and only if ... ?
 - Exclusive-or (XOR) gates: The output is 1 if and only if ... ?
 - Equivalence (XNOR) gates: The output is 1 if and only if ... ?
 - Comments on the logical symbols and logical connectives.

3.2 Exercise:

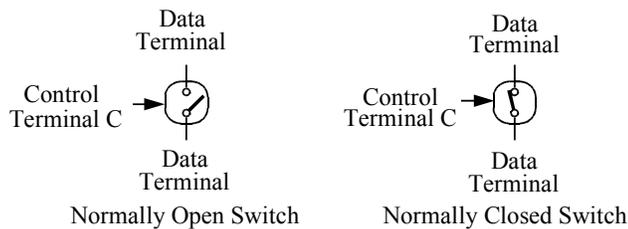
- Determine how many different two-input gates there can be. In other words, how many unique Boolean functions of two inputs can you construct?
- How many different three-input gates? Alternately, how many unique Boolean functions of three inputs can you construct?
- Generalize this

4 Building a structural model for gates

This section presents a very simple structural model of gates based on an idealized device called a *logic switch*.

4.1 Logic switches

- Definition: A logic switch is a three-terminal device that is used to control the connection of two points in a circuit.

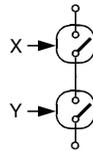


- Switch states:
 - Closed: Switch conducts between its data terminals.
 - Open: No conduction between the data terminals.
 - When $C=0$, the switch is in its normal state.
 - When $C=1$, the switch is in its active or on state.
 - When $C=1$, the arm is pulled towards the C input.

- Ideal switch assumption:
 - 0 resistance when closed, ∞ resistance when open.
 - 0 delay switching between open and closed.
- Real electronic switches are implemented with transistors, and they fail to meet the ideal switch assumptions in that:
 - Resistance in the open state is high, but not infinite.
 - Resistance in the closed state is low, but not zero.
 - Time required to change states is greater than zero.

4.2 Exercise:

- The following switch network conducts between its two terminals just in case both the signals X and Y are 1.

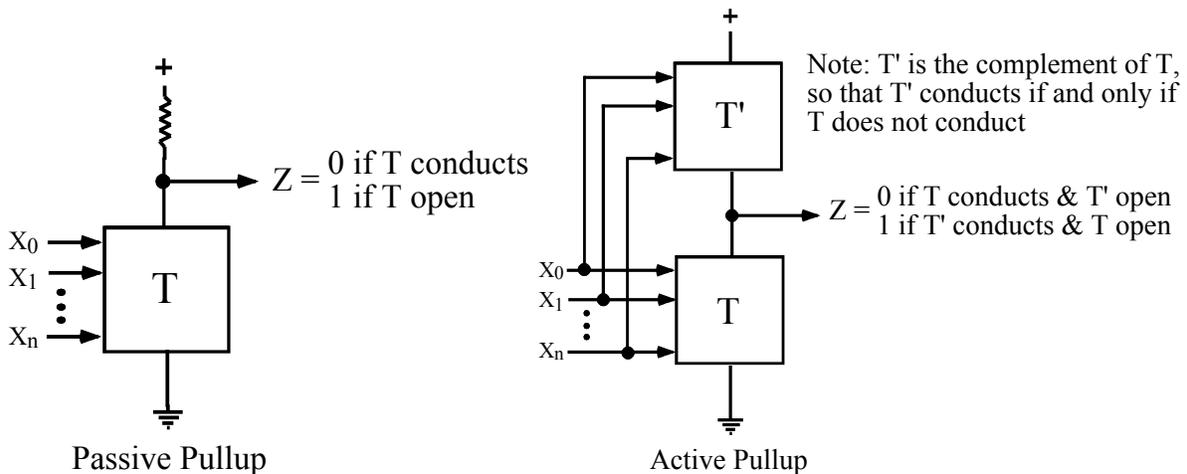


- Design three two-terminal networks, each with two control signals X and Y, such that the networks conduct only if:
 - Network 1: X is 1 or Y is 1.
 - Network 2: X is 1 and Y is 0.
 - Network 3: X and Y are equal

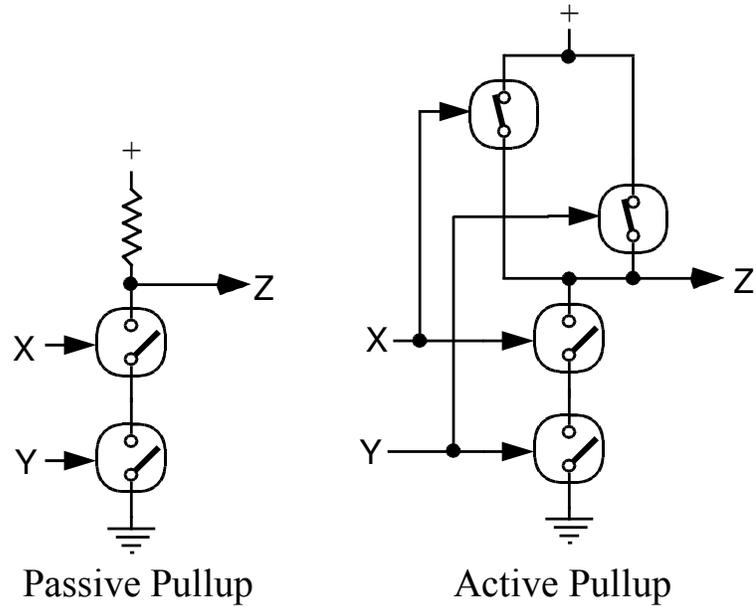
Let us look at switch implementations of inverters, nands, and nors.

4.3 General model

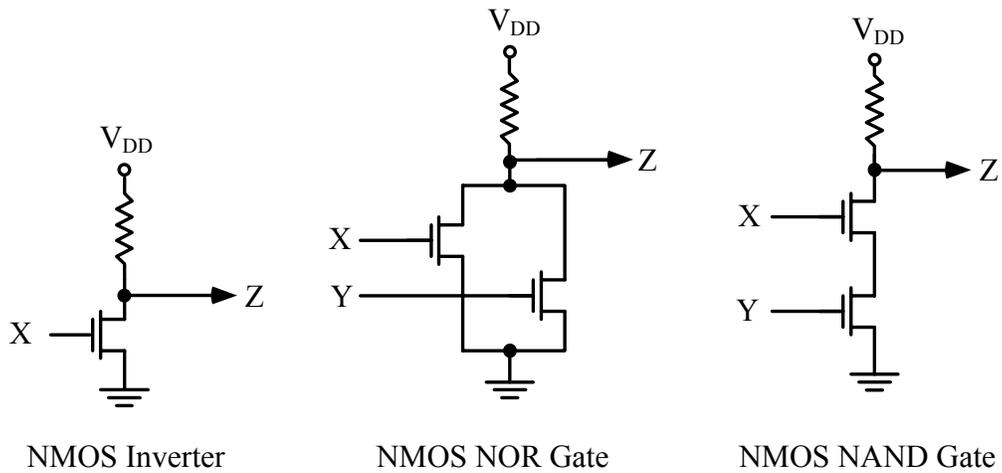
The general model for implementation of gates hinges on the use of *passive* versus *active* pullup

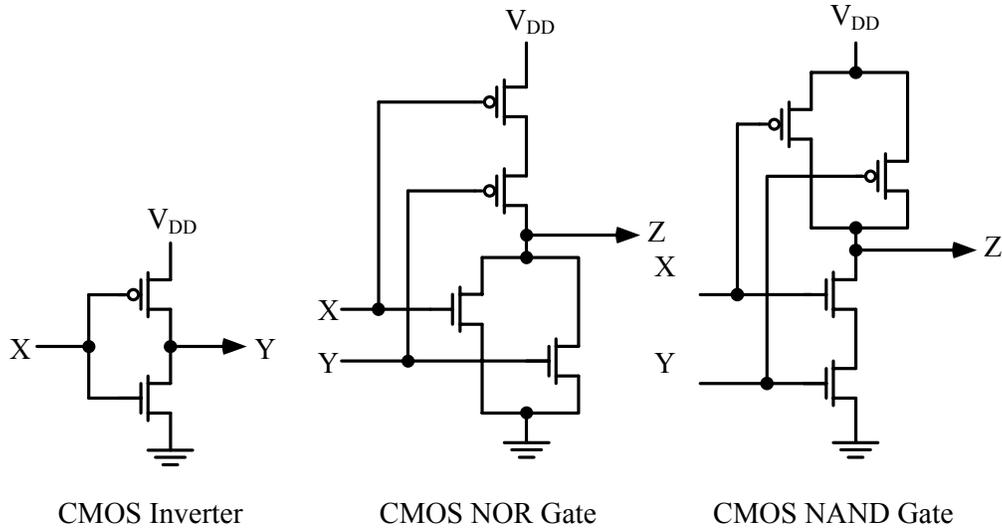


- The boxes labeled T and T' contain switches connected in such a way that they establish a connection between the top and bottom terminals when the input signals take on certain values and cause an open circuit if the input signals take on any other values.
- The two networks in the active pullup circuit must be designed so that they are never both conducting or are both open at the same time (recall the definition of complementary MOS).



5 nMOS and CMOS logic families



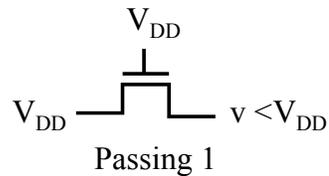
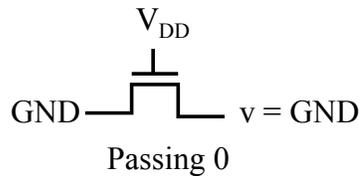


5.1 Properties of nMOS and CMOS gates

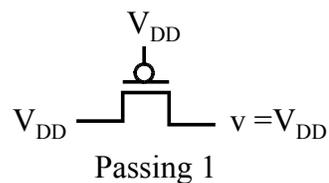
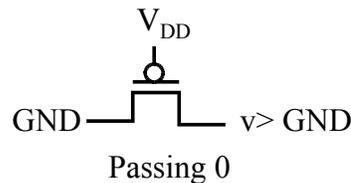
- No current flows through the gate unless the input signal is changing
- High input impedance
- High fanout
- Sandwich structure of MOS transistor creates capacitor between the gate and substrate
- High input capacitance that slows transition time (switching speed) and limits fanout
- nMOS dissipates power in low output state
- The faster a CMOS gate switches the more power it dissipates, so there is a tradeoff between speed and power
- CMOS gate only dissipates power when it is changing state (no longer true, ask me why)

5.2 Transmission gates

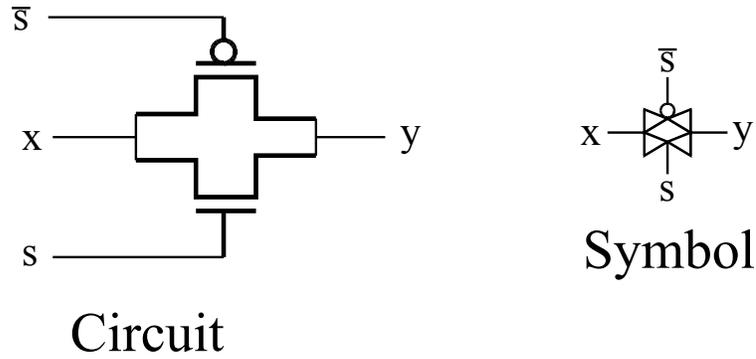
- Passing 0s and 1s through a MOS Transistor
- nMOS transistors pass a 0 better than a 1



- pMOS Transistors pass a 1 better than a 0



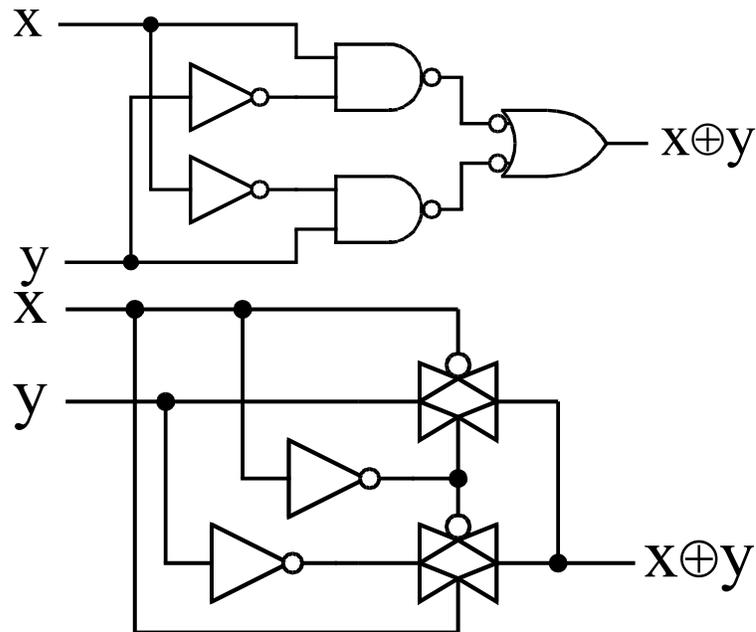
- This is the reason that nMOS transistors are used in the pull-down network and pMOS in the pull-up network of a CMOS gate. Otherwise the noise margin would be significantly reduced. We will look at noise margins in greater depth soon.
- A transmission gate is essentially a switch that connects two points. In order to pass 0's and 1's equally well, a pair of transistors (one nMOS and one pMOS) are used as shown below:



- When $s = 1$ the two transistors conduct and connect x and y
- The top transistor passes x when it is 1 and the bottom transistor passes x when it is 0
- When $s = 0$ the two transistor are cut off disconnecting x and y

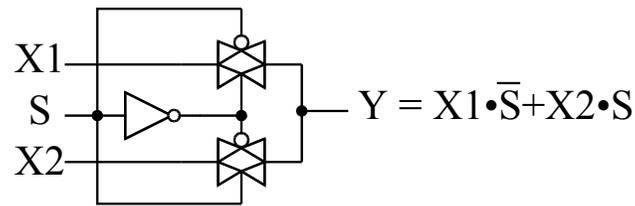
5.2.1 Implementing XOR gates

- With NAND gates and inverters:
- With transmission gates



- Why would one of these circuits be preferable to the other?

5.2.2 Implementing a multiplexer with transmission gates



- When $S = 0$, input X1 is connected to the output Y
- When $S = 1$, input X2 is connected to the output Y

5.3 Tri-state outputs

What happens when two wires are shorted?

- Instead of the usual two, these outputs have three possible states, 0, 1, and Z (high impedance)
- States 0 and 1 are standard logic levels
- State Z is called the high impedance output state. It is not a logic level.
- A tri-state gate is realized by adding a switch to the output of a regular gate. This switch is controlled by an external output control signal.
- When the output control signal is asserted, the switch is closed and the gate acts like a normal gate.
- When the output control signal is deasserted, the switch is open and the gate is disconnected from its output terminal.
- The switch on the output could be implemented by a transmission gate
- Is the control signal C asserted high or low? How would you change the circuit to assert it the other way?
- Tri-state buffers are the preferred way to implement buses.

6 Ideal vs. real gates

Some of the most important differences between real and ideal gates are due to the resistance of the real switches

- As discussed previously, a transistor switch has a small, but non-zero, resistance in the on state and a large, but not infinite, in the off state.
- This resistance has two major effects:
 1. The output voltages of the gates are adversely affected.
 2. The gates require non-zero time to switch states.

