Implementation of Channel Estimation and Multiuser Detection Algorithms for W-CDMA on Digital Signal Processors

Sridhar Rajagopal   Gang Xu   Joseph R. Cavallaro

Electrical & Computer Engineering Dept.
Rice University
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Outline

- Introduction to W-CDMA
- Use of DSPs in wireless communications
- Channel Estimation and Multistage Detection
- DSP implementation issues
- Real-time requirements
- Conclusions
Wideband-CDMA

- Third generation wireless communication systems
- Multimedia capabilities
- Multirate services
- Quality of service
- Higher Data Rates: 2 Mbps, 384 Kbps, 144 Kbps.
DSPs in Wireless Communications

- Digital Signal Processor
- Signal Processing \leftrightarrow Communications
- Prototyping advanced communication algorithms

Features:
- Low Power Consumption
- Low Cost
- High Performance
The Wireless Channel: Multiuser, Multipath

- Direct Path
- Reflected Paths
- Noise + MAI
- Antenna
- Desired User

Faces Attenuation, Delays and Doppler Effects: Unknown Channel Parameters
Base-Station Receiver

- Antenna
- Demodulator
- Demux
- Multiuser Detector
- Decoder
- Channel Estimator
- Estimated Amplitudes & Delays
- Data
- Pilot

TI DSPS FEST 1999
CDMA Uplink System

User 1
\(d_1\)

User 2
\(d_2\)

User K
\(d_K\)

Channel Encoder

Spreading

AWGN

\(+\)

Matched Filter

Matched Filter

Matched Filter

Multi-User Detector

Channel Decoder

Demux

\(y_1\)

\(y_2\)

\(y_K\)

\(R(t)\)
Maximum Likelihood - Channel Estimation

- Send a time-multiplexed Preamble (Pilot).
- Channel properties extracted from received signal.
- Compare received signal with known pilot and estimate channel parameters.
- Keep estimate for remaining data bits (static).
- Repeat preamble every frame, if no tracking.
The Maximum Likelihood Algorithm

- Compute the correlation matrices $R_{rr}, R_{br}$ & $R_{bb}$.
- Compute the channel estimate $Y = R_{br} R_{bb}^{-1}$.
- Calculate the noise covariance matrix $K$.
- Calculate the channel impulse response vector $z$.
- Extract the amplitudes and delays from the channel impulse response vector using least squares fit.
The ML Algorithm Complexity

- Complex-Real Dot Product.
  
- Complex-Real Matrix Product.

- Complex -Real Product.

- Real Square roots.
  - Solving quadratic equation for least squares fit.

- Critical code : Matrix-vector multiplications / Dot Product

\[
R_{br} = \frac{1}{L} \overline{b} \cdot \overline{r}
\]

\[
Y = R_{br} \left[ R_{bb}^{-1} \right]
\]

\[
Z^H_k = (y^H_{2k-1} U^R_k + y^H_{2k} U^L_k) \left( U^R_k U^R_k + U^L_k U^L_k \right)^{-1}
\]

TI DSPS FEST 1999  Assuming Unity Noise Covariance
Differencing Multistage - Multiuser Detection

- Based on the principle of Parallel Interference Cancellation (PIC)
- Cross-correlation information used to remove interference of other users from desired user
- Repeated iterations for convergence
- Differencing techniques applied for improving the performance of the algorithm
The Differencing Multistage Detector

- Split the crosscorrelation matrix into lower, upper and the diagonal matrix. \( R = D + S + S^T \)
- Calculate the channel impulse response iteratively using

\[
A_{Z}^{(l)} = A_{Z}^{(l-1)} - (S + S^T) A\hat{x}^{(l-1)}
\]

where \( \hat{x}^{(l-1)} = \hat{d}^{(l-1)} - \hat{d}^{(l-2)} \)

(\( \hat{x}_k \in \{0,+2,-2\} \))

- \( x \) is called the differencing vector.
Multistage Detector Complexity

- **Matrix Multiplication:** \( B = (S + S^T)A \)
  - Computed only once for one frame

- **Dot Product:**
  \[
  z_k^{l+1} = z_k^l - \sum B_{ij} \hat{x}_j^l
  \]
  - Computed iteratively

- **Critical code:** Dot Product
TI Tools Used

- Evaluation Modules (EVM) for C6201 and C6701 fixed and floating point DSPs
  - 64 KB each internal program & data memory
  - 256 KB SBSRAM, 8 MB SDRAM (external)
- C Compiler ver 3.0 from Code Generation Tools
- Code Composer ver 4.02 for profiling the code
DSP Implementation: Channel Estimation

- Floating point implementation found more feasible due to matrix inversions and square-roots.
- Code optimized for the DSP
- Use of Specialized approximate instructions
  - Approximate reciprocal square roots
  - Approximate reciprocals
- Use of Assembly Code for critical part.
  - TI's C67 floating point benchmarks for Matrix-Vector Multiplication & Dot Product
- Data Memory requirements for Channel Estimation
Use of Approximate Instructions

<table>
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<th>TMS320C67x DSP</th>
<th>Cycles</th>
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<tr>
<td>Approx. FP Reciprocal Sq. root Instruction</td>
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</tr>
<tr>
<td>FP Reciprocal Sq. root Instruction</td>
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L = 150, P = 3, N = 31,
SNR = 5dB, SINR = -10 dB

10% improvement

100% improvement
Optimization Effects for Channel Estimation

Effect of optimizations for Channel Estimation on C6701-->

- Base (-o3 -pm)
- Approx. (-o3 -pm with intrinsics) 1.08X improvement
- Assembly opt. (-o3 -pm with asm) 2.34X improvement

Execution time(normalized) -->
Data Memory Requirements

Data to be placed in External memory

Data Memory Requirements for Multiuser Channel Estimation

Number of Users: 6, 130

Preamble Length: 5, 120
DSP Implementation: Multistage Detection

- 16-bit Fixed Point C Code
- Code optimized for the DSP
- Use of Assembly Code for critical part
  - TI's C62 fixed point assembly benchmarks for Dot Product
- Data memory requirements for Multistage Detection
Optimization Effects for Multistage Detector

Effect of optimizations for Multistage Detection on C6201 -->

Global opt. 
(-o3 -pm -mu)

5.22X improvement

Software Pipelining
(-o3 -pm)

7.47X improvement

Assembly opt. 
(-o3 -pm with asm)
Data Memory Requirements

Data can be placed completely in Internal memory.
2X speedup for a three-stage detector

Flops Count

Users: K=15  SNR=6dB

Conventional Method
Differencing Method

2X speedup for a three-stage detector
Real-Time Requirements

Real-Time capability by C6201 DSP

![Graph showing the comparison between Conventional Method and Differencing Method under SNR=10dB WindowSize=12.]

- **Conventional Method**
  - 8 users: 310 kb/s
  - 12 users: 150 kb/s

- **Differencing Method**
  - 8 users: 350 kb/s
  - 12 users: 190 kb/s

**Note:** The graph shows that the Differencing Method significantly reduces the maximum bit rate per user compared to the Conventional Method, especially as the number of users increases.
Trends in Recent DSPs

- More internal memory and higher clock speeds
  - C6203: 512 KB data, 384 KB program, 250 MHz
  - useful for uplink channel estimation algorithms.

- Specialized Blocks in the DSP Core.
  - Viterbi decoding in C54.

- Lower Voltage operation
  - 1.2 V in C5402, useful for saving power consumption in the mobile.
Conclusions

- Implementation issues: Estimation & Detection Algorithms
- Channel Estimation - Floating Point / External Memory
- Multistage Detection - Fixed Point / Internal Memory
- Specialized instructions: square root/reciprocals.
- Additional support for complex arithmetic useful.
- Recent trends in DSPs highly encouraging for next generation wireless communication applications.
Future Work

- Effect of caches & DMA Controllers
  - C6211 (4KB each L1 Program & Data, 64 KB L2)

- DSP implementations for W-CDMA uplink and downlink
  - Blind Algorithms
  - Adaptive Algorithms

- Architectural bottlenecks and compiler issues in DSPs to enhance suitability for next generation W-CDMA systems.