DSPs for future wireless systems

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Abstract

This abstract presents the research activities at Rice University regarding the mapping of physical layer baseband processing algorithms onto architecture designs. We are exploring ASIC, FPGA and DSP-based architectures to implement several sophisticated baseband algorithms proposed for future wireless systems. The data rate requirements for future wireless systems has increased by orders-of-magnitude (from Kbps to several Mbps), requiring more sophisticated algorithms for their implementation. Apart from the increase in data rates, future wireless systems also need additional flexibility both at the base-station and at the mobile handset. The base-station needs to support multiple users and varying parameters for each user, such as the spreading gain, the constraint lengths for decoding and possibly, channel-dependent algorithms. The mobile may also need to switch between these parameters and also between standards. Although the data rate requirements can be met by exploiting more parallelism in ASICs or FPGAs, these do not lead to flexible, scalable or production-friendly systems. An implementation on current generation DSPs, however, does not provide the computational horsepower needed for these algorithms.

We are exploring DSP-based architecture solutions by analyzing the bottlenecks in the algorithms on an architecture simulator (the Imagine simulator). The cycle accurate simulator provides the base Imagine architecture (a VLIW-based media processor with 48 functional units) and allows us freedom to explore the architecture space. We are investigating real-time architecture design issues such as the number of functional units needed, functional unit design and utilization, data access from memory and issues in sequential traceback occurring during Viterbi decoding. Since we are implementing the algorithms on a parallel architecture, we are also examining the overhead in communication against computation time. Alternative and complementary solutions, such as reconfigurable architectures and FPGA implementations for Viterbi-Turbo decoding, handset architectures and a joint simulation-prototyping testbed for W-LAN and W-CDMA, are also being studied in our research group. The ASIC and FPGA implementations are then used as reference points for area-time-power tradeoffs against the proposed DSP-based architecture solution. Though our initial goal is a real-time design, further investigation would include low-power implementation issues. The innovations and ideas leading from this research can then be integrated into future DSP architectures.